MOTOROLA INC.
Communications Sector

MSF 5000™ & PURC 5000™ WILDCARD MODULE

OPTIONS C232AA, AB, AG AND C233AB: FACTORY INSTALLED
MODEL QLN2914A: FIELD INSTALLED

1. OPTION BREAKDOWN CHART

Option	*Previous	*Present	Description	Change
C232AA	—	—	DC Remote Control Wildcard	—
	TRN5175A	TRN9754A	Wildcard Module	Added
	TRN9118A	TRN9118A	Escutcheon	Replaces TRN5954A
	TKN8985A	TKN8985A	Cable Kit	Added
C232AB	—	—	Tone Remote Control Wildcard	—
C232AG	TRN5175A	TRN9754A	Wildcard Module	Added
C233AB	TRN9118A	TRN9118A	Escutcheon	Replaces TRN5954A
	TKN8985A	TKN8985A	Cable Kit	Added
QLN2914A	—		Field Modification Kit	—
	TRN5175A	TRN9754A	Wildcard Module	Added
	TRN9118A	TRN9118A	Escutcheon	Added
	TKN8985A	TKN8985A	Cable Kit	Added
TLN4151	—	—	**Field Installed Relay Kit	—

*Both kit models are current.

**Refer to instruction section 68P81101E71 for details.

2. DESCRIPTION

2.1 The factory installed Option C232 consists of a Wildcard Module installed in the Expansion Tray of an MSF 5000™ Base Station. It provides the system with the capability of controlling external devices, and also has the ability to process inputs from the same or other external devices. The Wildcard Module is used to signal an external device, via the forward wildcard function, when a specific bit is detected on the MUXbus, or it will write data onto the MUXbus, via the reverse wildcard function, when a signal is received from an external device. The wildcard can be configured with up to four circuit board mounted dual form-C relays for closure control of external devices such as lights or alarms. The Wildcard Module is also available as a Field Modification Kit.

2.2 A wide variety of non-standard Wildcard Module configurations are available by using jumpers in different positions. A description of these options and appropriate jumpers (installed as field modifications) is given in the Field Modifications paragraphs.

2.3 The Wildcard Module, whether a factory or a field installation, is installed in the optional Expansion Tray. An OPERATE/RESET switch (S1301) is provided for maintenance purposes. Four circuit board mounting areas are available for the optional (field installable) relays. Also, transistor switched grounds are available (from Q1301 through Q1304) at J1302-17, -11, -5, and -2, respectively.

2.4 Extra solder pads are available on the circuit board to field install jumper wires to select optional signals and controls. The factory installed "standard" jumpers are shown by solid lines on the schematic diagram. The optional jumper positions are described in the schematic notes and in the Field Modifications paragraphs.

2.5 The Wildcard Option may be used in either DC remote control or tone remote control stations. When a C232 option is factory installed in a DC remote control station, the station control code plug is default programmed at the factory to allow remote control of forward wildcard signals FWC1 and FWC2. DC remote control supports only two FWC parameters. Refer to Table 1. When a C232 option is factory installed in a tone remote control station, the tone remote control code plug is default programmed at the factory to allow remote control of forward wildcard signals FWC1 through FWC4. Refer to Table 2. Field installation of the Wildcard Option also requires that a properly programmed code plug be obtained via the Model QLN2914A Wildcard Field Modification Kit.

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1/7/87-UP

NOTE

A C233 option is physically identical to a C232 option. However, no code plug programming is provided and the C233 option acts as a MUXbus interface only.

2.6 The Model TRN9754A Wildcard Module is designed to accept the plug-on installation of secondary boards, via connectors J1303, J1304, and J1305. The purpose of the secondary boards is to add specific predefined capabilities to the existing I/O control of external devices provided by the Widlcard Module. The Model TRN9754A Wildcard Module provides selective jumpering of power, ground, and I/O lines to the secondary board, as required to enable it to perform its specific task.

NOTE

The Model TRN5175A Wildcard Module does not provide the secondary board plug-on capability of the Model TRN9754A. Otherwise, both wilcards provide the same I/O control of external devices.

2.7 Refer to the attached schematic diagram of the Model TRN9754A Wildcard Module for specific details of the selective jumper interconnections provided to the secondary board via connectors J1303, J1304, and J1305.

Table 1. DC Remote Control Standard Default Conditions

Function	FWC1	FWC2	FWC3	FWC4
After Reset or Power Up.	On	Off	**	**
DC Current —5.5 mA	Off	On	**	**
DC Current + 12.5 mA	On	Off	**	**

**FWC3 and FWC4 are not used with this option.

Table 2. Tone Remote Control Standard Default Conditions

Function	FWC1	FWC2	FWC3	FWC4
After Reset or Power Up.	On	Off	On	Off
Function Tone 1050 Hz	X	X	Off	On
Function Tone 1150 Hz	X	X	On	Off
Function Tone 1250 Hz	Off	On	X	X
Function Tone 1350 Hz	On	Off	X	X

X = Remains as in previous state.

3. INSTALLATION

3.1 A Wildcard Module is intended to be mounted inside of an optional Expansion Tray, which is racked on top of the station control tray. The module's position inside the Expansion Tray is determined by what other optional modules are installed. As shown in Figure 1, these positions are numbered one, two, and three, from right to left, starting next to the Power Supply Module.

3.2 Install the Wildcard Module in accordance with the following steps.

Step 1. Remove AC (or DC) power from the station. Proceed to Step 8 if the Expansion Tray and Power Supply are already installed.

Step 2. Open the cabinet and slide the RF Tray and Station Control Trays forward.

Step 3. Remove small cover, near top center of Station Control Tray lid, to expose the 40-pin expansion connector (J800).

Step 4. Snap the Expansion Tray to the top of the Station Control Tray.

Step 5. Install Expansion Tray Power Supply Module in the right-hand position in the Expansion Tray. Secure the board in the tray by installing the Power Supply escutcheon (see Figure 1).

Step 6. Lay the 40-pin expansion cable in the adapter tray and connect the center connector (P800) to the 40-pin expansion connector J800 on the station control board. Refer to Figure 1 and connect the right-hand end (P1701) to the power supply (J1701). Fasten the left end in place using the two screws provided in the field modification kit. The left end is now defined as the expansion tray connector J1700.

Step 7. The 34-conductor options cable has 4 connectors. One end of this cable will have 2 connectors that are approximately 2 inches apart. Insert the connector that is located about 2 inches in from that end of the cable into the 34-pin options cable connector (J1702) on the power supply board. Place the protective paper over both ribbon cables, between the power supply board and the Expansion Tray connector J800.

Step 8. Install the Wildcard Module in position one (next to the power supply) if that position is available. If not, install the wildcard in the next available position. If the wildcard is installed in position two, draw the middle connector of the options cable through the slit in the protective paper and connect it to the Wildcard Module.

Step 9. Connect the options cable from the power supply (or option card) to connector J1301 on the Wildcard Module. Install the front panel wildcard escutcheon.

Step 10. Route the 25-conductor wildcard cable (W1301) through the hinge area of the Expansion Tray and connect it to J1302 on the Wildcard Module and close the expansion tray cover. Fold cable W1301 so it lays flat against the back of the Expansion Tray and place cable W1301 in the hooks on the back of the Expansion Tray. It may be necessary to remove the Expansion Tray cover in order to install cable W1301.

Step 11. Connect the free end of the cable W1301 to the appropriate connector on the junction box in the following manner: feed the ribbon cable under the RF Tray

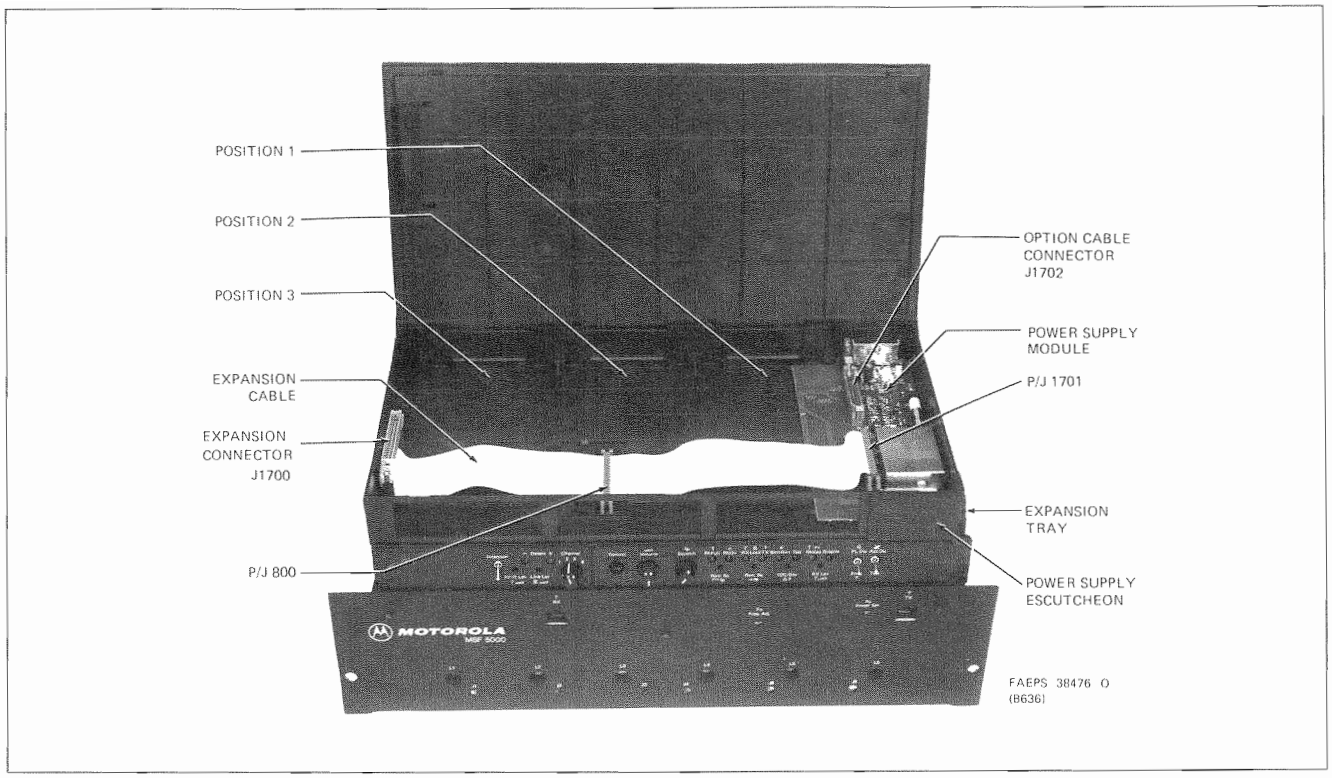


Figure 1. Expansion Tray Layout

slides and rail on the right hand side of the station before attaching it to the junction box. The 25-conductor cable (W1301) is assembled with 2 folds of cable that are secured with cable wraps. If the option card is in position one, install the cable as described previously with the free end of the cable mounted into position J1 on the junction box. If the option card is in position two, one of the folds in cable W1301 must be unfolded before connecting the free end of the cable to position J2. If the option card is in position three, both folds in the cable will have to be loosened before connecting the free end of the cable to position J3.

Step 12. Push the RF Tray back in place and secure it.

4. THEORY OF OPERATION

4.1 GENERAL

4.1.1 As shown in the block diagram (Figure 2), the wildcard module receives an input address (BA0-BA3) from the MUXbus in the base station that controls the function to be performed. This function will result in either a forward or reverse wildcard action. The input data (BD0-BD3) on the data bus contains the specific details of the function performed. The reset and data strobe circuits provide timing and control signals to assist in performing a specific function.

4.1.2 When a forward wildcard address is received by address decoder U1301 and U1302 and wildcard address driver U1305, the input data on the data bus is accepted by flip-flops U1313 and U1314 which control relay driver circuits Q1301 thru Q1304 and relays K1301 thru K1304. When a reverse address is received by the address decoder U1301 and U1302 and by the reverse address driver U1315, the data bus control gate U1304 will allow the reversed inputs from external devices to be conditioned and gated onto the data bus. The data bus carries the information to the base station.

4.2 FORWARD WILDCARD OPERATION
(Refer to Schematic Diagram and Figure 3)

4.2.1 The input address from the MUXbus cycles continuously through address BA0 thru BA3 and is applied to the 1-of-8 decoders/multiplexers U1301 and U1302. The address is applied through non-inverting buffers U1303 to isolate the decoders from the MUXbus. Address BA3 is low to select decoder U1301 and high to select decoder U1302. As the address cycles through, all decoder outputs A0 thru A15 go low for the duration of the individual address (approximately 310 microseconds

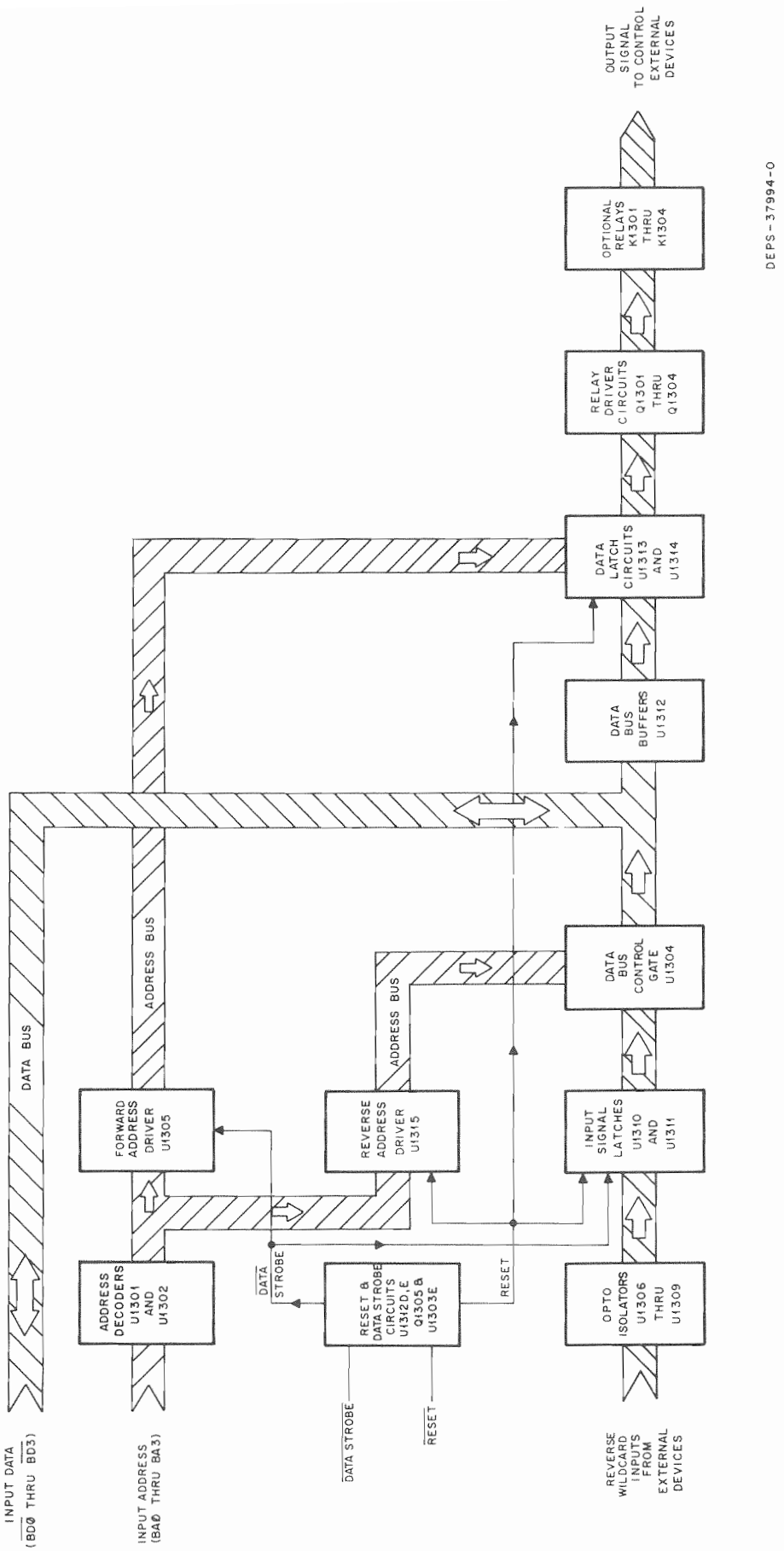


Figure 2. Wildcard Module Block Diagram

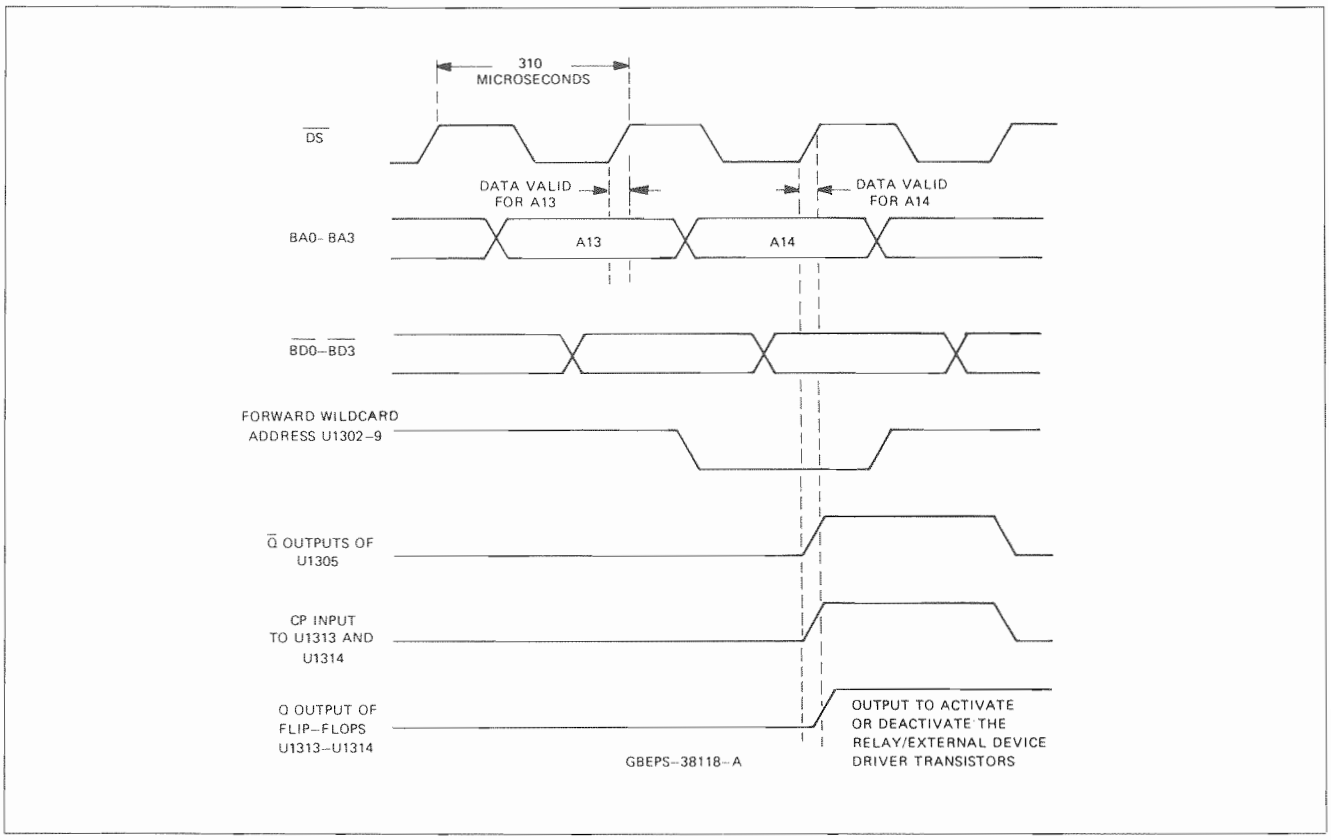


Figure 3. Forward Wildcard Timing Diagram

per address). One of the decoder outputs (usually A14) is selected by jumper JU101 (on TRN5175A) or JU107 (on TRN9754A) to control forward wildcard address driver U1305.

4.2.2 Jumpers JU8 thru JU10 are used to connect all inputs to the forward wildcard address together if it is desired for one address from the MUXbus to control all relay drivers. When the decoder output is low at inputs D0 thru D3 of address driver U1305 and the forward edge of the data strobe signal (DS) is rising, the address driver outputs Q0 thru Q3 will go high and are applied to relay driver flip-flops U1313 and U1314 at their respective CP inputs.

4.2.3 Input data BD0-BD3 from the MUXbus is inverted by bus buffers U1312 and applied to the D input of relay driver flip-flops U1313 and U1314. Jumpers JU26 thru JU30 can be rearranged if it is desired for the input data to control separate relay driver flip-flops.

4.2.4 The relay driver flip-flops U1313 and U1314 will be set (Q output high) only when the D input is high and the CP input is rising from low to high. If the input data high signal arrives at the D input of U1313 and U1314 after the CP address input has already toggled high, the flip-flop will not be set until the address bus BA0 thru BA3 cycles to A14 again, which is a delay of approximately 5 milliseconds.

4.2.5 Jumpers JU33 thru JU36 and JU43 thru JU46 are used to select which output of the relay driver flip-flops are used (usually Q output) to control transistors Q1301 thru Q1304. When the Q output is high, the transistor will be turned on to supply a ground path for the external device. If installed, relays K1301 thru K1304 will be energized when transistors Q1301 thru Q1304 are turned on. Jumpers at the transistor and/or relay outputs can be arranged to select the desired control of the external device.

4.2.6 The DS signal is buffered from the MUXbus by U1303E and is used to properly gate the selected forward wildcard address when the DS at the CP input of address driver U1305 rises from low to high, a condition that occurs approximately every 310 microseconds. The falling (high to low) portion of the data strobe is used during reverse wildcard functions.

4.2.7 The RESET signal from the MUXbus is placed on the expansion bus by the Station Control Module, and affects the operation of the entire base station. The reset signal from OPERATE/RESET switch (S1301) is used to disable the wildcard operation only. Both reset

signals function in the same manner in the Wildcard Module. The reset signal applies a low to relay driver flip-flops U1313 and U1314 (CD input), applies a high, via U1312E to reverse wildcard address driver gates U1315, and applies a low to the CD inputs of input pulse latches U1310 and U1311. The reset signal prohibits forward wildcard signals from controlling an external device, prohibits data from being put on the data bus, when a reverse wildcard input occurs, and resets the input signal latches U1310 and U1311.

4.3 REVERSE WILDCARD OPERATION
(Refer to Schematic Diagram and Figure 4)

4.3.1 Just as described for the Forward Wildcard Operation, the input address from the MUXbus is applied to U1301 and U1302. another of the outputs (usually A13) is selected by jumper JU102 (on TRN5175A) or jumper JU108 (on TRN9754A) to control reverse wildcard address driver U1315. When the input address BA0 thru BA3 sets output Q5 (A13) of decoder U1302 low, the reverse wildcard address driver U1315 will provide a high signal to data bus control gates U1304. Jumpers JU1 thru JU7 are usually arranged to allow the A13 decoder output to be applied to all NOR gates of U1315 but the jumpers can be arranged so that each NOR gate uses a separate address from the decoder if desired. The output of data bus control gates U1304 will go low when a high reverse wildcard data signal (RWD1 thru RWD4) is received from the input pulse latch which represents an external device input.

4.3.2 When the switch on an external device is activated, a ground is supplied which allows current to flow through the optoisolator (U1306 thru U1309). Jumpers JU57 thru JU72 are used to select the method the external device uses to signal the optoisolator. A current of approximately 20 milliamps activates the optoisolator which supplies a low signal to the SD input of pulse latch U1310 and U1311. With the $\overline{SD}$ input low the Q output will be high. The Q outputs of U1310 and U1311 are the reverse wildcard data (RWD1 thru RWD4) inputs that are applied to the data bus control gates U1304. RWD1 thru RWD4 will stay high until the SD input goes high and the latch CP input receives the next falling edge of the data strobe.

4.3.3 The output of the applicable data bus control gates U1304 goes low, when an external device is activated, and when the decoded Reverse Wildcard address signal is sent from U1315. The data bus control gate then writes a bit on the data bus which is transferred to the base station via the MUXbus.

4.3.4 Three different modes for operating the input pulse latches U1310 and U1311 can be selected with jumpers JU20, 21, 24, 25, 39, 40, 47 and 48. The modes are: (1) non-latched signaling, (2) latched signaling with cross-reset, and (3) latched signaling with external reset.

4.3.4.1 NON-LATCHED SIGNALING

The non-latched signaling mode uses the wildcard to provide each of the four external devices a separate and independent path to communicate Reverse Wildcard (RWC) Inputs 0 through 3 back to the base station. The input latches U1310 and U1311 are normally in a reset state until set by an input. The input latches reset again when the input is removed. Table 3 shows the inputs and outputs during operation. A timing diagram of the signals is shown in Figure 4.

4.3.4.2 LATCHED SIGNALING, WITH CROSS-RESET

The latched signaling with cross-reset mode is selected by removing jumpers JU25 and 48 and installing jumpers JU20, 21, 24, 39, 40, and 47. This mode divides the

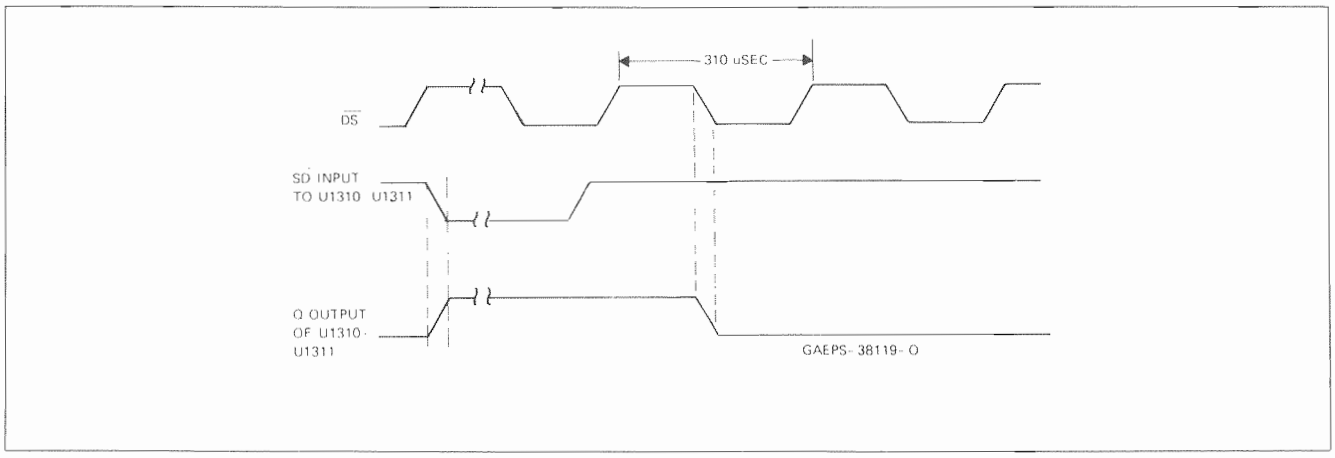


Figure 4.
Reverse Wildcard Input (Non-Latched) Timing Diagram

Table 3. Non-Latched Signaling Truth Table

Inputs			Outputs		
SD	CD	K	Q	Q	Condition
H	L	X	L	H	After system reset—By station or local reset
H	H	H	L	H	Normal—Waiting for a RWC Input
L	H	X	H	L	Set—When a RWC Input is received
H	H	H	L	H	Reset—When RWC Input is removed

H = HI; L = LO; X = Don't Care.
Jumpers JU20, 21, 24, 39, 40 and 47 OUT. Jumpers JU25 and 48 IN.

input circuits into two separate pairs. RWC Inputs 0 and 1 to U1310 as one pair, and RWC Inputs 2 and 3 to U1311 as the other. The purpose of each pair is to latch the received input signal after an RWC Input (0 or 2) is received and keep it latched until the other RWC Input (1 or 3) is received. The inputs and outputs of one pair (U1310A and B) are shown in Table 4 (both pairs function identically). A timing diagram of the signals is shown in Figure 5.

Table 4.
Latched Signaling, with Cross-Reset Truth Table

Inputs (Pin)						Outputs		
2	3	16	7	8	12	15	11	
SD_1	CD_1	K_1	SD_2	CD_2	K_2	Q_1	Q_2	Condition
H	L	X	L	H	X	L	H	After System Reset—By station or local reset
H	H	H	H	H	L	L	H	Normal—Waiting for RWC Input 0 or 2
L	H	X	H	H	H	H	H	Set latch 1— RWC Input 0 or 2 received
H	H	L	H	H	H	H	L	Latched state— RWC Input 0 or 2 removed
H	H	L	L	H	X	H	H	Reset latch 1/Set latch 2 — RWC input 1 or 3 received
H	H	H	H	H	L	L	H	Latched State—Waiting for RWC Input 0 or 2

H = HI; L = LO; X = Don't Care
Jumpers JU20, 21, 24, 39, 40, and 47 IN. Jumpers JU25 and 48 OUT.

4.3.4.3 LATCHED SIGNALING, WITH EXTERNAL RESET

The latched signaling via external reset mode is only used when it is desired to have an input signal remain latched as long as the K input(s) of input signal latches U1310 and U1311 are grounded. With the K input low, the RWC Input will set the latch, which will remain in the set state (latched) until either a RESET signal is received via the Expansion bus, or via the wildcard OPERATE/RESET switch S1301, forcing the K input to go high. The inputs and outputs of input signal latches U1310 and U1311 are shown in Table 5.

Table 5.
Latched Signaling, with External Reset Truth Table

Inputs			Outputs		
SD	CD	K	Q	Q	Condition
H	L	L	L	H	After System Reset—By station or local reset
H	H	L	L	H	Normal—Waiting for a RWC Input
L	H	L	H	L	Set—RWC Input received
H	H	L	H	L	Latched—RWC Input removed
H	H	H	L	H	Reset—Enable external reset switch
H	H	L	L	H	Latched—External reset switch disabled

H = HI; L = LO; X = Don't Care.
Jumpers JU20, 21, 24, 39, 40 and 47 OUT. Jumpers JU25 and 48 IN.

5. MAINTENANCE

Maintenance of the Wildcard Module consists of performing the troubleshooting procedures shown in the troubleshooting chart and checking logic signals in accordance with the timing diagrams. Use standard chip handling practice for removal and installation of components.

6. FIELD MODIFICATIONS

6.1 GENERAL

6.1.1 Field modifications can be made to the Wildcard Module by using the special jumper capability of the printed circuit board. The standard jumper configurations, installed by the factory, are shown as solid jumper lines on the schematic diagram.

6.1.2 The special jumpers are listed and described in the following paragraphs. Some examples are given using partial circuit diagrams from the schematic diagram that can be used to determine the complete circuit functions.

NOTE
The factory installed jumpers are all "stand-up" zero-ohm resistors, except for the two address decoder output jumpers (which are wires). Field installed jumpers should be wires.

6.2 REVERSE WILDCARD ADDRESS DRIVER (U1315) INPUTS

The following special jumper usage information is only applicable when these "normally out" jumpers are installed.

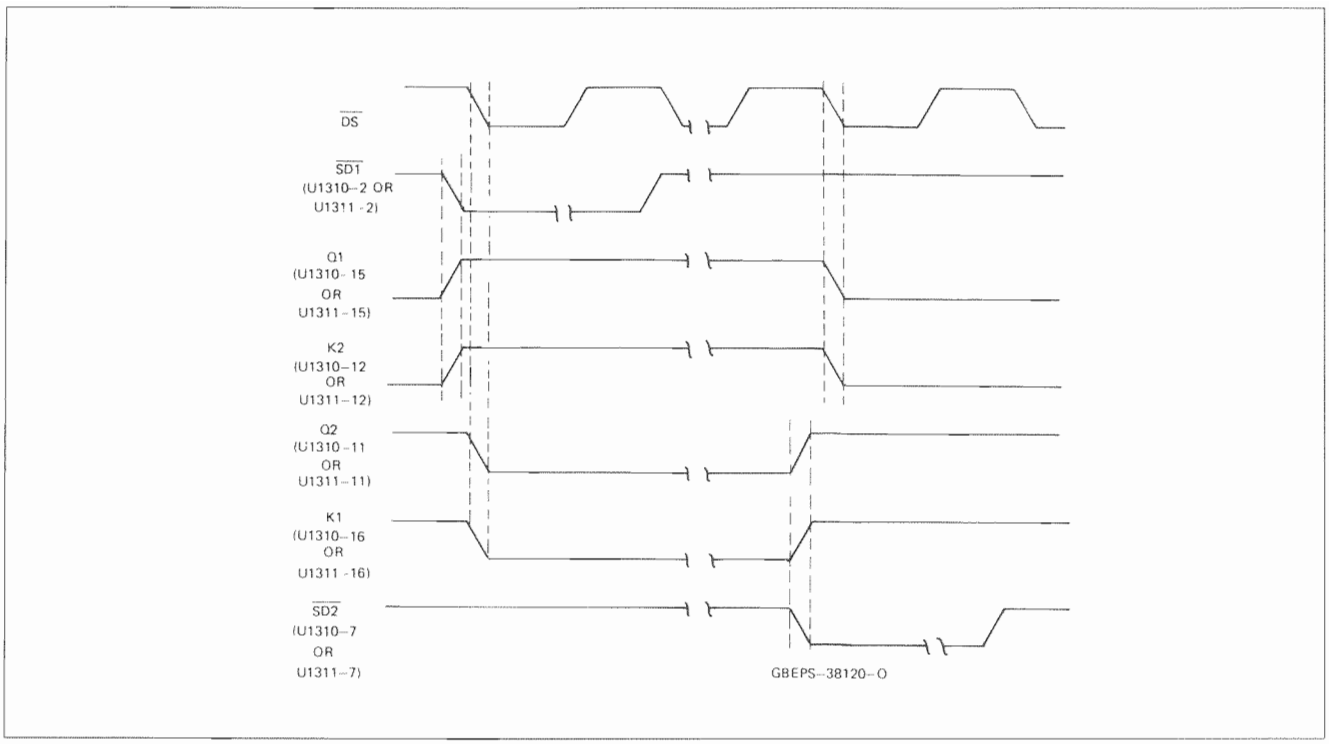


Figure 5.
Latched Signaling, with Cross-Reset Timing Diagram

JU4 Prevents U1315A-2 from floating low when it is NOT desired to have the reverse wildcard data input RWD1 signal gated onto the MUXbus. When JU4 is installed, none of the MUXbus decoded address lines (from U1301 or U1302) should be tied to U1315A-2.

NOTE

If any of the four reverse wildcard address inputs of U1315 are allowedto float low, the result would allow any reverse wildcard input (RWD1 thru RWD4 or RWD1 thru RWD4) that might be active to be gated onto the MUXbus, whenever the input(s) to U1315 went low.

In applications of the Wildcard Module where it is desired to disable all reverse wildcard inputs, remove reverse wildcard address select jumper JU102 (on TRN5175A) or JU108 (on TRN9754A) and install JU4, 5, 6, and 7. This will ensure that the wildcard will not signal the MUXbus that a reverse wildcard input has occurred.

JU5 Prevents the input of U1315B-5 from floating low when it is NOT desired to have the reverse wildcard data input RWD2 signal gated onto the MUXbus. When JU5 is installed, none of the MUXbus decoded address lines (from U1301 or U1302) should be tied to U1315B-5.

JU6 Prevents the input of U1315C-8 from floating low when it is NOT desired to have the reverse wildcard data input RWD3 signal gated onto the MUXbus. When JU6 is installed, none of the MUXbus decoded address lines (from U1301 or U1302) should be tied to U1315C-8.

JU7 Prevents the input of U1315D-11 from floating low when it is NOT desired to have the reverse wildcard data input RWD4 signal gated onto the MUXbus. When JU7 is installed, none of the MUXbus decoded address (from U1301 or U1302) should be tied to U1315D-11.

6.3 REVERSE WILDCARD DATA BUS CONTROL GATE (U1304) OUTPUTS

The following special jumper usage information is only applicable when these "normally out" jumpers are installed.

JU11, 12, 13 These jumpers allow more than one reverse wildcard input signal to be jumpered to one of the four MUXbus data lines BD0 thru BD3 by using either JU4, JU5, JU6 or JU7. See Figures 6 and 7. Also refer to Table 6.

CAUTION

When jumpers JU11, 12 and/or JU13 are used, care must be taken in the selection of data bus jumpers JU4 thru JU7 to prevent two or more data lines from being shorted together.

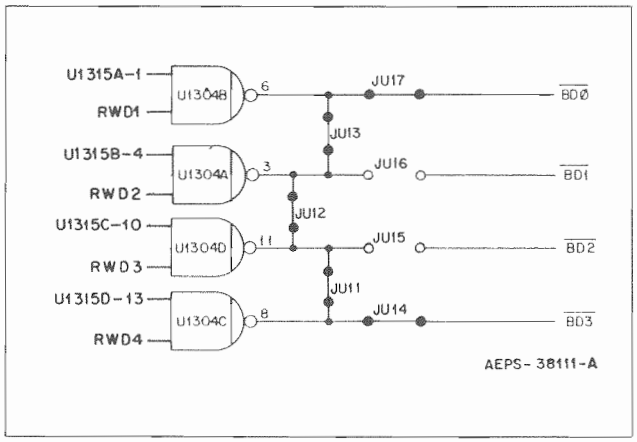


Figure 6.
Example of Incorrect Jumpering

CAUTION

In Figure 6, the desire is to signal the MUXbus via BD0. Notice, however that data lines BD0 and BD3 are shorted together via JU11, 12, and 13. This condition will cause a station malfunction, since two data lines are shorted together. To correct the problem of Figure 6, two solutions are possible. Remove JU12, which would allow either a RWD1 or RWD2 input to signal MUXbus bit BD0. Also, RW3 and RW4 would signal the MUXbus via BD3.

OR

Remove JU14. This would allow any of the four RWD inputs to signal MUXbus bit BD0 only.

6.4 FORWARD WILDCARD DATA BUS BUFFER (U1312) OUTPUTS

The following special jumper usage information is only applicable when these "normally out" jumpers are installed.

JU30, 31, 32 When all three jumpers are used, any one of the four MUXbus data lines BD0-BD3, can be used (via JU26-JU29) to provide the signal that will activate or deactivate the relay driver circuitry. See examples in Figure 8 and 9.

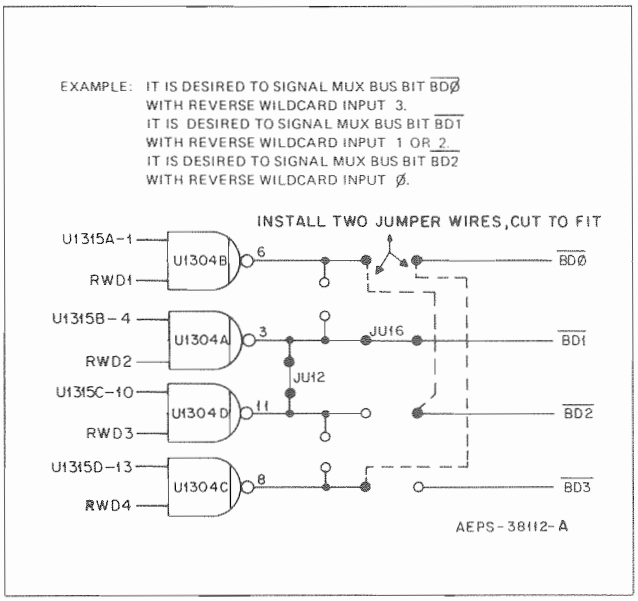


Figure 7.
Example of a Possible Field Modification

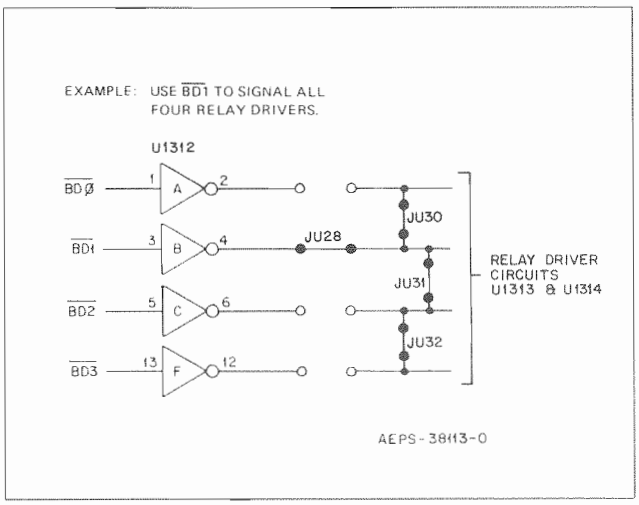


Figure 8.
BD1 to Signal All Four Relays

6.5 REVERSE WILDCARD INPUTS VIA J1302

The following special jumper usage information is only applicable when these "normally out" jumpers are installed.

JU67 Reverse Wildcard Input 0. Used when desired to provide an external voltage to activate the optoisolator, instead of the +13.8 V or +5 V available from the wildcard. When an external supply is used, JU68 must be removed. Then, R1301 must be recalculated so that the input current ($I_{forward}$) through optoisolator U1306 is approximately 20 mA.

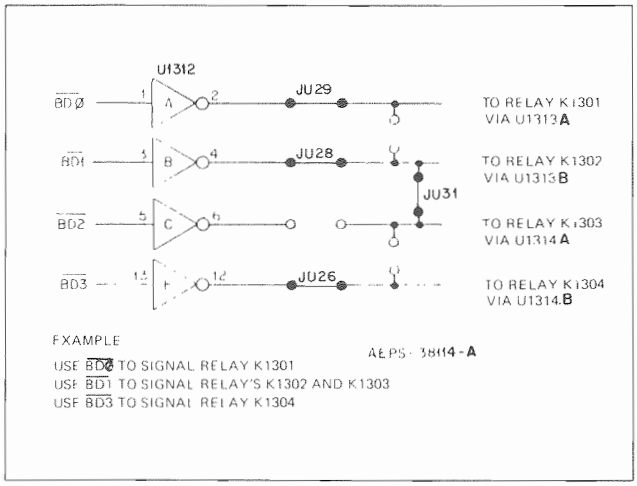


Figure 9.
Input Data to Signal Diffrent Relays

JU65 Reverse Wildcard Input 1. Same as for JU67. When JU65 is used, then JU66 is removed, and R1302 is changed to allow approximatley 20 mA of forward current through optoisolator U1307.

JU69 Reverse Wildcard Input 2. Same as for JU67. When JU69 is used, then JU70 is removed, and R1303 is changed to allow approximately 20 mA of forward current through optoisolator U1308.

JU71 Reverse Wildcard Input 3. Same as for JU67. When JU71 is used, then JU72 is removed, and R1304 is changed to allow approximately 20 mA of forward current thru optoisolator U1309.

JU57 Provides an internal ground path for Reverse Wildcard Input 0 (+). Used in cases where the external device signals the wildcard via JU67, but does not provide the return path. Also, remove JU58.

JU59 Provides an internal ground path for Reverse Wildcard Input 1 (+) via JU65. Also, remove JU60.

JU61 Provides an internal ground path for Reverse Wildcard Input 2 (+) via JU69. Also, remove JU66.

Table 6. Examples of Jumpering a Reverse Wildcard Data Input Onto the MUXbus

Desired Operation		JU11	JU12	JU13	JU14	JU15	JU16	JU17
1) Reverse Wildcard Input 0 to Signal MUXbus Line BD0.	Factory Installed, See Note	OUT	OUT	OUT	OUT	OUT	OUT	IN
2) Reverse Wildcard Input 1 to Signal MUXbus Line BD1.	Factory Installed See Note	OUT	OUT	OUT	OUT	OUT	IN	OUT
3) Reverse Wildcard Input 2 to Signal MUXbus Line BD2.	Factory Installed See Note	OUT	OUT	OUT	OUT	IN	OUT	OUT
4) Reverse Wildcard Input 3 to Signal MUXbus Line BD3.	Factory Installed See Note	OUT	OUT	OUT	IN	OUT	OUT	OUT
5) All reverse Wildcard Inputs (0-3) to Signal MUXbus Line BD0.	Field Installed or modified	IN	IN	IN	OUT	OUT	OUT	IN
6) All reverse Wildcard Inputs (0-3) to Signal MUXbus Line BD1.	Field installed or modified	IN	IN	IN	OUT	OUT	IN	OUT
7) All reverse Wildcard Inputs (0-3) to Signal MUXbus Line BD2.	Field installed or modified	IN	IN	IN	OUT	IN	OUT	OUT
8) All reverse Wildcard Inputs (0-3) to Signal MUXbus Line BD3.	Field installed or modified	IN	IN	IN	IN	OUT	OUT	OUT
9) Reverse Wildcard Inputs 0 and 1 to Signal MUXbus Line BD0.	Field installed or modified	OUT	OUT	IN	OUT	OUT	OUT	IN
10) Reverse Wildcard Inputs 2 and 3 to Signal MUXbus Line BD3.	Field installed or modified	IN	OUT	OUT	IN	OUT	OUT	OUT
11) Reverse Wildcard Inputs 1 and 2 to Signal MUXbus Line BD1.	Field installed or modified	OUT	IN	OUT	OUT	OUT	IN	OUT
12) Reverse Wildcard Inputs 1 and 2 to Signal MUXbus Line BD2.	Field installed or modified	OUT	IN	OUT	OUT	IN	OUT	OUT

NOTE: Examples 1 thru 4 are factory installed on each wildcard. The remaining versions and any other combinations are modified in the field.

JU63 Provides an internal ground path for Reverse Wildcard Input 3 (+) via JU71. Also, remove JU64.

CAUTION

Again, as with the reverse wildcard input MUXbus jumpering, care must be taken to insure that two or more data lines are not tied together as shown in Figure 10.

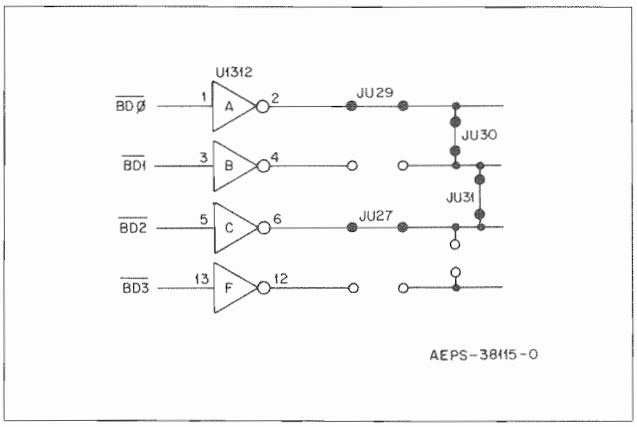


Figure 10.
Example of Incorrect Jumpering

6.6 RELAY OUTPUTS VIA K1301 THRU K1304

The following special jumper usage information is only applicable when these "normally out" jumpers are installed.

JU56 When the first relay option is installed, jumper JU92 is removed and JU56 is added. This jumper provides the normally closed path for section-A of relay K1301, via external connector J1302-17. Factory installed jumpers JU89 and JU91 provide the normally open and wiper arm portions, respectively, of relay K1301A.

JU54 When a second relay option is installed, jumper JU87 is removed and JU54 is added. This jumper provides the normally closed path for section-A of relay K1302, via external connector, J1302-11. Factory installed jumpers JU84 and JU86 provide the normally open and wiper arm portions, respectively, of relay K1302A.

JU52 When a third relay option is installed, jumper JU82 is removed and JU52 is added. This jumper provides the normally closed path for section-A of relay K1303, via external connector JU1302-5. Factory installed jumpers JU79 and JU81 provide the normally open and wiper arm portions, respectively, of relay K1303A.

JU50 When a fourth relay option is installed, jumper JU77 is removed and JU50 is added. This jumper provides the normally closed path for section-A of relay K1304, via external connector J1302-2. Factory installed jumpers JU74 and JU76 provide the normally open and wiper arm portions, respectively, of relay K1304A.

JU55, 88, 90 These jumper positions are provided as a means of utilizing the B-section of relay K1301. They may be connected, for example, to control a circuit in the custom circuit area provided at the front of each wildcard board.
JU55 is a normally open relay contact.
JU88 is a normally closed relay contact.
JU90 is the wiper arm of the B-section.

JU53, 83, 85 These jumper positions perform the same function as JU55, 88 and 90, but are used with the B-section of relay K1302.
JU53 is a normally open relay contact.
JU83 is a normally closed relay contact.
JU85 is the wiper arm of the B-section.

JU51, 78, 80 These jumper positions perform the same function as JU55, 88 and 90, but are used with the B-section of relay K1303.
JU51 is a normally open relay contact.
JU78 is a normally closed relay contact.
JU80 is the wiper arm of the B-section.

JU49, 73, 75 These jumper positions perform the same function as JU55, 88 and 90, but are used with the B-section of relay K1304.
JU49 is a normally open relay contact.
JU73 is a normally closed relay contact.
JU75 is the wiper arm of the B-section.

6.7 POWER SUPPLY OPTIONS

The custom circuit areas of each Wildcard Module (see Figures 11 and 12), offer the user some board area so that a "custom made" circuit can be installed. There is also space provided for two potentiometers and one LED.

6.7.1 TRN5175A Wildcard Custom Circuit Areas

To provide circuit flexibility, the Model TRN5175A Wildcard provides a set of jumper locations to connect the +5 V, +9.6 V and +13.8 V supply voltages to the modules custom circuit areas. Refer to Figure 11. In addition, a jumper location is provided so that the user can

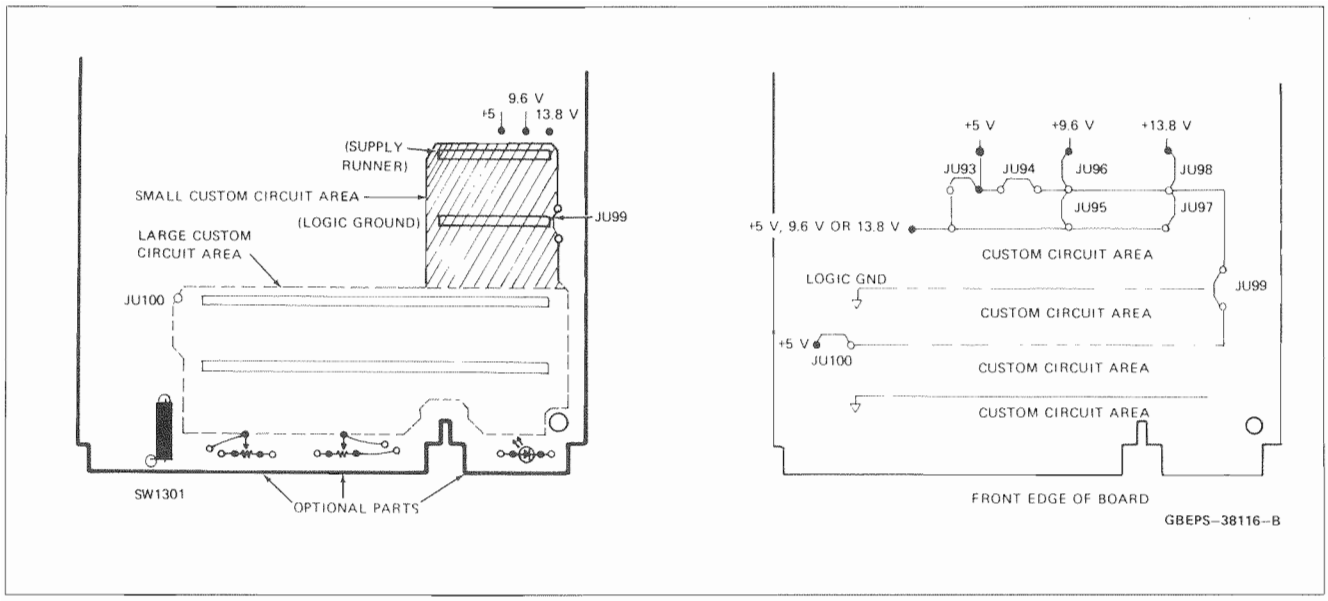


Figure 11. TRN5175A Wildcard Custom Circuit Area Jumpering

provide two of the three available voltages to the circuits (i.e., +5 V for logic IC's, +9.6 V or +13.8 V for an op amp circuit). Refer to Tables 7 and 8.

It is also possible to utilize various Expansion Bus I/O lines that are present at J1301. Plated-torugh holes are provided next to J1301, and are intended to be jumpered into the custom circuit area. These holes are intended for custom applications, and will not be described here. Refer to the Jumper Table, provided on the schematic diagram, for specific information concerning the jumpers available for the custom circuit areas.

6.7.2 TRN9754A Wildcard Custom Circuit Area

To provide maximum circuit flexibility, the Model TRN9754A Wildcard provides a set of jumper locations to connect either the +5 V, +9.6 V, or +13.8 V supply voltage to the module's custom circuit area. Also, the Wildcard provides for the plug-on installation of a secondary circuit board, via J1303, J1304, and J1305. Refer to Figure 12.

In addition, jumper locations are provided so that the user can select either Logic or Audio ground for use in the custom circuit area. Refer to Table 9.

It is also possible to utilize various Expansion Bus I/O lines that are present at J1301. Plated-through holes are provided next to J1301, and are intended to be jumpered into the custom circuit area. These holes are intended for custom applications and are not described here. Refer to the Jumper Table provided on the schematic diagram for specific information concerning the jumpers available for the custom circuit area.

6.8 FLIP-FLOP CROSS RESET (U1310, 1311) JUMPERS

The following special jumper usage information is only applicable when these "normally out" jumpers are installed.

JU39, 40, 47 — These three jumpers are used when it is desired to have U1310A and B Reverse Wildcard Inputs cross-reset each other. Jumper JU48 must be removed, and when operating with this cross-reset scheme, use Reverse Wildcard Inputs 0 and 1.

The cross-resetting operation can be observed on a Diagnostic Metering Panel (DMP). Upon station power-up, or after a

Table 7. Power Supplied to Entire TRN5175A Wildcard Custom Circuit Areas (Note 1)

Voltage	JU93	JU94	JU95	JU96	JU97	JU98	JU99	JU100
+5 V (note 2)	OUT	IN	OUT	OUT	OUT	OUT	IN	OUT
+9.6 V	OUT	OUT	OUT	IN	IN	OUT	IN	OUT
+13.8 V	OUT	OUT	IN	OUT	OUT	IN	IN	OUT

NOTES:
1. In the custom circuit area of the board it is possible to provide either +9.6 V or +13.7 V as a power supply voltage to one part of the circuit area and a second voltage to the other portion. See Table 8.
2. Jumpers JU99 and JU100 will provide the same results.

reset (either station or wildcard generated), input data latch U1310 will reset reverse wildcard data line 1 (RWD1 will become a logic 1), and set reverse wild card data line 2 (RWD2 will become a logic 0).

The result, as seen on a DMP, will show LED "RWC5" as being off (reset), and LED "RWC6" as being on (set). The next input signal received at Input 0 will cause RWD1 to be set, and RWD2 to be reset.

Table 8. Power Supplied to Selected TRN5175A Wildcard Custom Circuit Areas

Voltage	JU93	JU94	JU95	JU96	JU97	JU98	JU99	JU100
+5 V To Large Circuit Area, and +9.6 V To Small Circuit Area	OUT	OUT	OUT	IN	IN	OUT	OUT	IN
+5 V To Small Circuit Area, and +9.6 V To Large Circuit Area	IN	OUT	OUT	IN	OUT	OUT	IN	OUT
+5 V To Large Custom Circut Area, and +13.8 V To Small Custom Circuit Area	OUT	OUT	IN	OUT	OUT	IN	OUT	IN
+5 V To Small Custom Circuit Area, and +13.8 V To Large Custom Circuit Area	IN	OUT	OUT	OUT	OUT	IN	IN	OUT

Table 9. Power and Ground Supplied to TRN9754A Wildcard Custom Circuit Area

Voltage/Ground	JU93	JU94	JU95	JU97	JU100
+5 V	IN	OUT	OUT	XX	XX
+9.6 V	OUT	IN	OUT	XX	XX
+13.8 V	OUT	OUT	IN	XX	XX
Logic GND	XX	XX	XX	OUT	IN
Audio GND	XX	XX	XX	IN	OUT

XX = Don't care

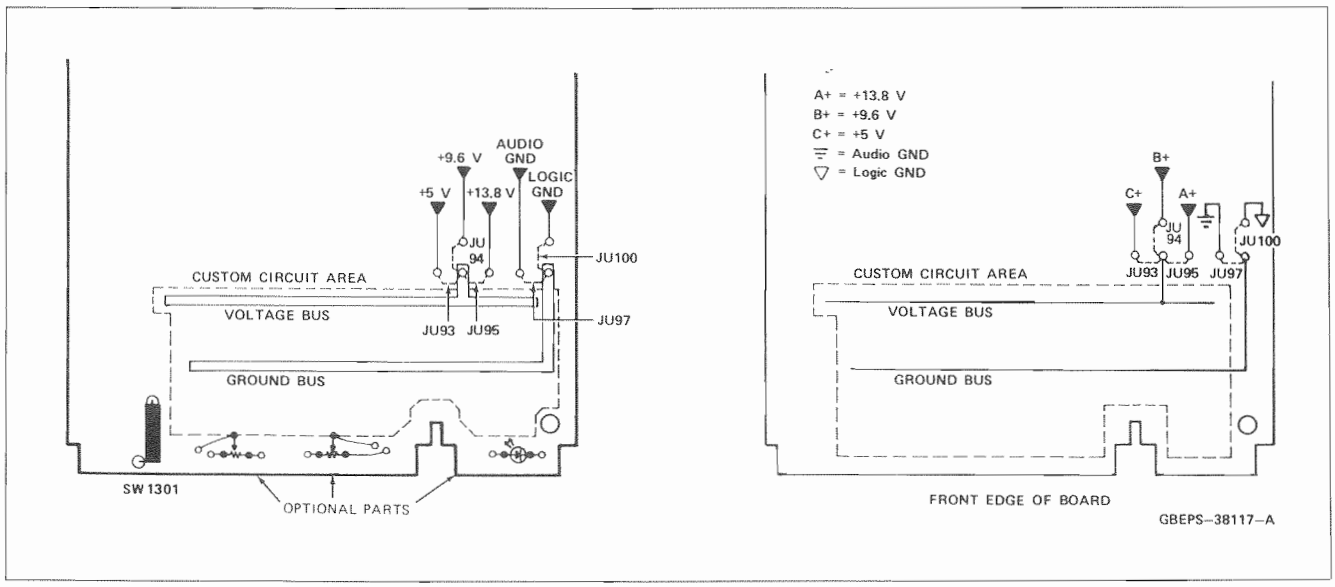


Figure 12. TRN9754A Wildcard Custom Circuit Area Jumpering

JU41 This jumper allows RWD1 to be provided to the Wildcard data bus, via U1304B. Jumper JU42 (RWD1) must be out. Hence, a DMP will show LED "RWC5" on, and LED "RWC6" off, until a Reverse Wildcard Input is received at Input 0. Then, a DMP will show LED "RWC5" off, and LED "RWC6" on.

JU37 This jumper allows RWD2 to be provided to the Wildcard data bus, via U1304A. Jumper JU38 (RWD2) must be out. Hence, a DMP will show LED "RWC6", on and LED "RWC5" off, until a Reverse Wildcard Input is received at Input 1. Then, a DMP will show LED "RWC6" off, and LED "RWC5" on.

JU20, 21, 24 These three jumpers are used when it is desired to have U1311A and B Reverse Wildcard Inputs cross-reset each other. Jumper JU25 must be removed, and when operating with this cross-reset scheme, use Reverse Wildcard Inputs 2 and 3.

The cross-resetting operation can be observed on a DMP. Upon station power-up, or after a reset (either station or wildcard generated), input data latch U1311 will reset reverse wildcard data line 3 (RWD3 will become a logic 1), and set reverse wildcard data line 4 (RWD4 will become a logic 0).

The result, as seen on a DMP, will show LED "RWC7" as being off (reset), and LED "RWC8" as being on (set). The next input signal received at Input 2 will cause RWD3 to be set and RWD4 to be reset.

JU22 This jumper allows RWD3 to be provided to the Wildcard data bus, via U1304D. Jumper JU23 (RWD3) must be out. Hence, a DMP will show LED "RWC7" on, and LED "RWC8" off, until a Reverse Wildcard Input is received at Input 2. Then, a DMP will show LED "RWC7" off, and LED "RWC8" on.

JU18 This jumper allows RWD4 to be provided to the Wildcard data bus, via U1304C. Jumper JU19 (RWD4) must be out. Hence, a DMP will show LED "RWC8" on, and LED "RWC7" off, until a Reverse Wildcard Input is received at Input 3. Then, a DMP will show LED "RWC8" off, and LED "RWC7" on.

6.9 FLIP-FLOP OUTPUT JUMPERS

The following special jumper usage information is only applicable when these "normally out" jumpers are installed.

JU45 Jumper JU45 allows the Q output of D flip-flop U1313A to be used to control relay driver transistor Q1301, instead of the normally used Q output, via jumper JU46. Jumper JU46 must be removed.

Using JU45 to control Q1301 results in it being normally on, thus keeping relay K1301 activated. Relay K1301 remains activated until either reset by the system (RESET), or by the wildcard (S1301), or by a MUXbus signal (BD0-BD3) to the wildcard.

JU36 Same as for JU45, buffer relay driver Q1302 and relay K1303. When JU36 is used, JU35 must be removed.

JU43 Same as for JU45, but for relay driver Q1303 and relay K1303. When JU43 is used, JU44 must be removed.

JU34 Same as for JU45, but for relay driver Q1304 and relay K1304. When JU34 is used, JU33 must be removed.

6.10 MUXbus ADDRESS DECODER (U1301 and U1302) OUTPUTS

The following special jumper usage information is only applicable when these "normally out" jumpers are installed.

NOTE

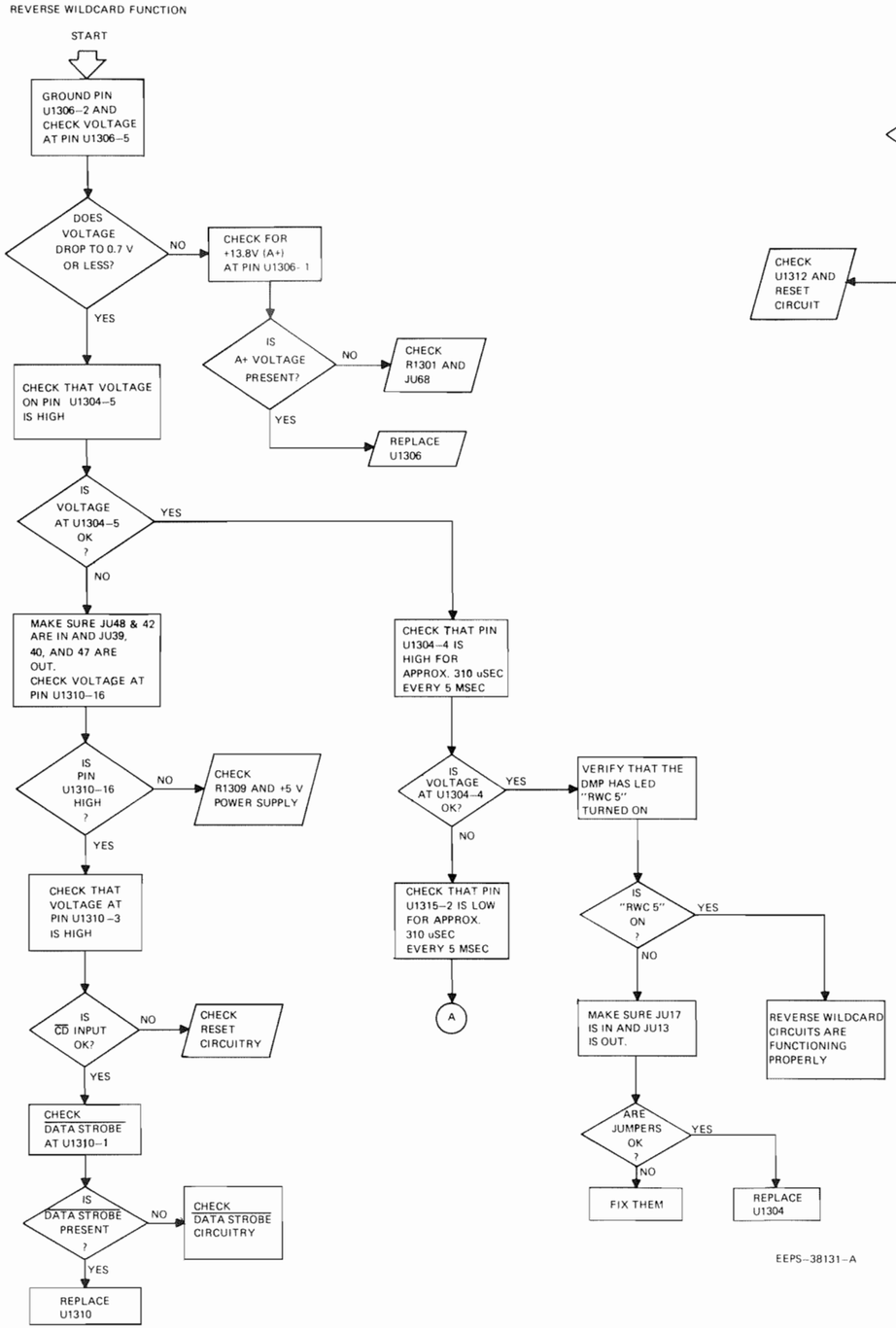
The decoded address outputs employ cut-to-fit wire jumpers to provide the user with flexibility of signal routing to the inputs of either the Forward or Reverse Wildcard Address Drivers (U1305 and/or U1315).

A0 thru A15 Address decoders U1301 and U1302 are binary 1-of-8 types that provide up to eight decoded addresses each. U1301 decodes addresses A0 thru A7. U1302 decodes addresses A8 thru A15.

Any of these available address lines can be jumpered to provide a different forward or reverse wildcard function. As shipped from the factory, the wildcard uses A13 for addressing reverse wildcard inputs, and address A14 for addressing forward wildcard inputs. However, any of the available address lines could be used for that purpose.

WILDCARD MODULE
MODEL TRN5175A
MOEEL TRN9754A

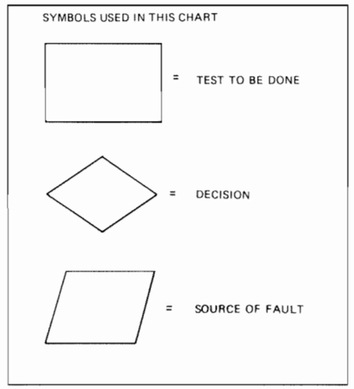
REVERSE WILDCARD FUNCTION



EEPS–38131–A

NOTES:

1. ALL VOLTAGE MEASUREMENTS ARE DC UNLESS OTHERWISE SPECIFIED.
2. A HIGH IS A VOLTAGE BETWEEN +2.5 V AND 5.25 V AND A LOW IS LESS THAN +0.7 V.
3. REFER TO THE SCHEMATIC DIAGRAM IN THIS MANUAL FOR VARIOUS CIRCUITS REFERENCED IN CHART.
4. THIS CHART IS FOR STANDARD JUMPER CONFIGURATION. THE TROUBLESHOOTING PROCEDURE MUST BE ADJUSTED IF NON–STANDARD JUMPERS ARE USED.
5. THIS CHART COVERS ONE OF THE FOUR SIMILAR CIRCUITS. THE CIRCUITS ARE THE SAME EXCEPT FOR THE IC NUMBERS.
6. JU101 FOR TRN5175A
   JU108 FOR TRN9754A
7. JU102 FOR TRN5175A
   JU107 FOR TRN9754A



parts list

TKN8985A Wildcard Cable Kit — PL-9323-A

REFERENCE NUMBER	MOTOROLA PART NO.	DESCRIPTION
W1301	30-83466P01	CABLE, flat w/CONNECTOR; 26-wire
	42-83553G01	STRAP, mounting; 5 used
	43-10646A09	STANDOFF; 2 used

TRN9118A Escutcheon Kit — PL-9324-O

REFERENCE NUMBER	MOTOROLA PART NO.	DESCRIPTION
	13-84202N03	BEZEL

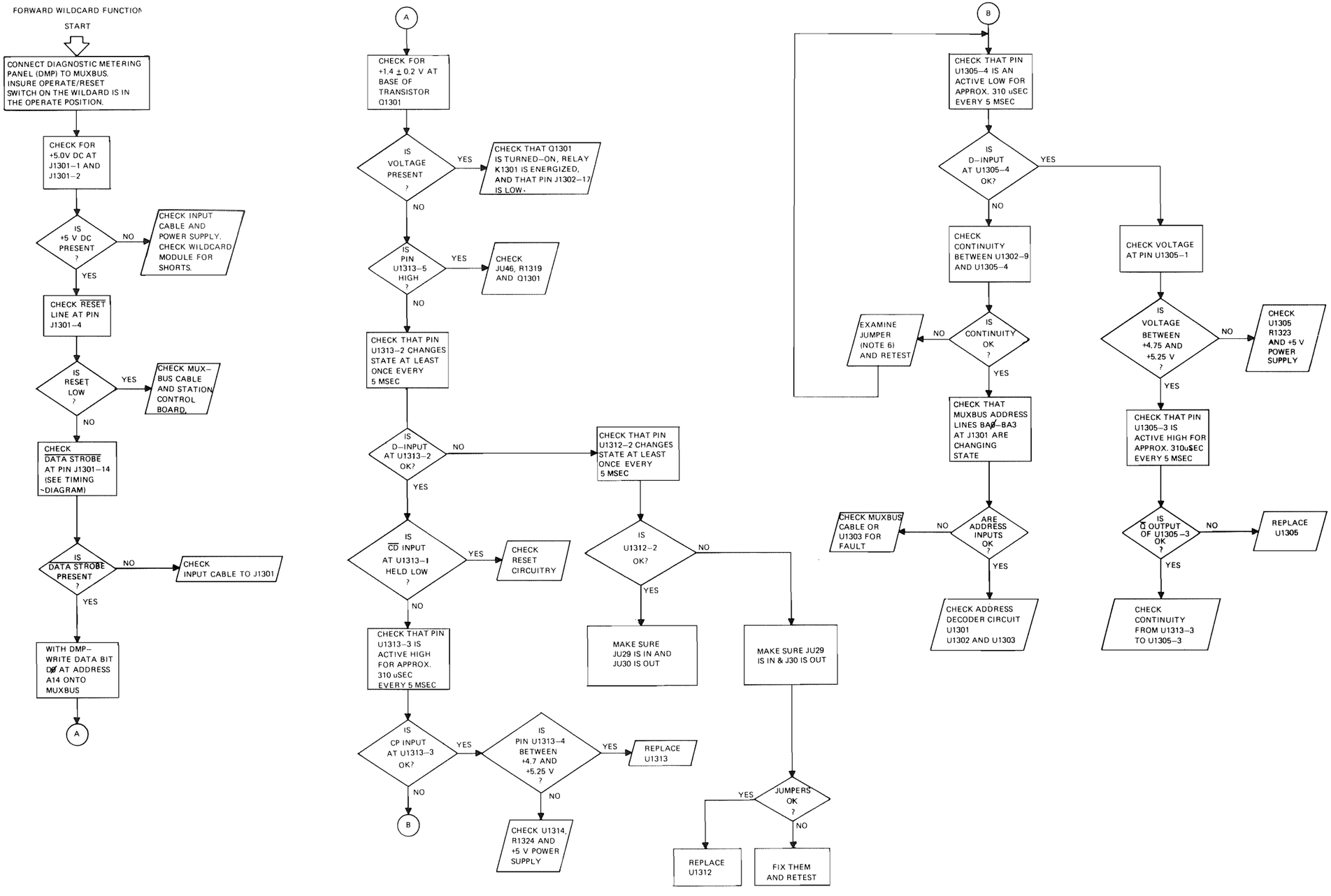
TLN4151A Relay Kit (Optional) — PL-455-C

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		diode: (see note)
CRxxx (see schematic)	48-82392B03	silicon (reverse voltage protection)
		relay, armature:
Kxxx (see schematic)	80-84201A01	2 form-C; coil res. 200 ohms
		non-referenced items
	43-84920H01	SPACER, relay

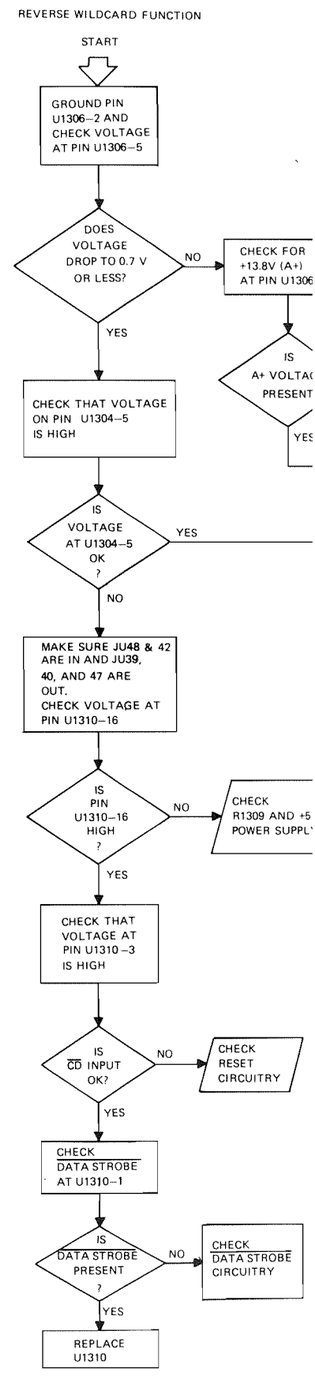
note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.

Troubleshooting Chart, and General Use Parts Lists
Motorola No. ***PEPS-41864-O***
3/29/85- UP

FORWARD WILDCARD FUNCTION



REVERSE WILDCARD FUNCTION



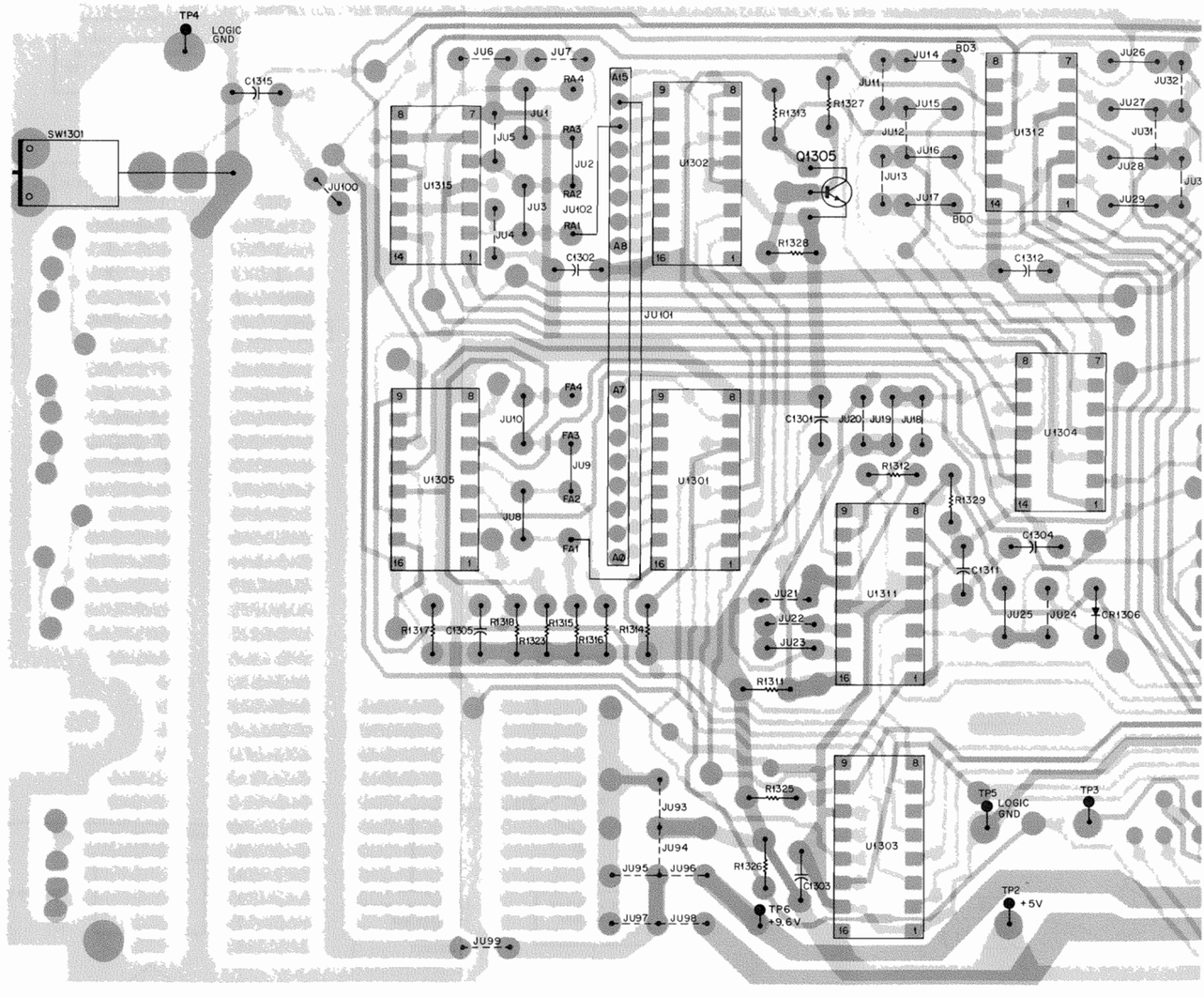
WILDCARD MODULE
MODEL TRN5175A

parts list

TRN5175A Wildcard Board — PL-8726-B

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed:
C1301 thru 1305	21-11021G07	.01 uF + 100-0%; 50 V
C1306 thru 1309	8-11017B07	.0068 uF ± 10%; 100 V
C1310 thru 1315	21-11021G07	.01 uF + 100-0%; 50 V
		diode: (see note)
CR1305, 1306	48-11034D01	silicon
		connector, receptacle:
J1301	28-83136N05	male; 34-contact
J1302	28-83136N01	male; 26-contact
		transistor: (see note)
Q1301 thru 1305	48-869706	NPN; type M9706 (Darlington)
		resistor, fixed: ± 5%; 1/4 W: unless otherwise stated
R1301 thru 1304	6-11009E44	620
R1305 thru 1312	6-11009E73	10k
R1313	6-11009E49	1k
R1314	6-11009E73	10k
R1315 thru 1318	6-11009E89	47k
R1319 thru 1322	6-11009E51	1.2k
R1323, 1324	6-11009E73	10k
R1325, 1326	6-11009E89	47k
R1327	6-11009E59	2.7k
R1328	6-11009E73	10k
R1329, 1330	6-11009E89	47k
R1331 thru 1334	6-11009E69	6.8k
		switch:
S1301	40-83685N12	spdt
		integrated circuit: (see note)
U1301, 1302	51-84561L41	binary address decoder
U1303	51-84561L77	hex tri-state buffer
U1304	51-84371K83	quad NAND gate
U1305	51-82609M73	quad D-type flip-flop
U1306 thru 1309	51-83629M75	opto-isolator
U1310, 1311	51-84561L88	dual JK flip-flop
U1312	51-84561L03	hex inverter
U1313, 1314	51-84561L34	dual D-type flip-fllop
U1315	51-84561L06	quad 2-input NOR gate
		mechanical parts
	6-11009F23	JUMPER, zero ohm resistor; 44 used
	29-10271A15	PIN, test; 6 used (TP1 thru 6)

note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.

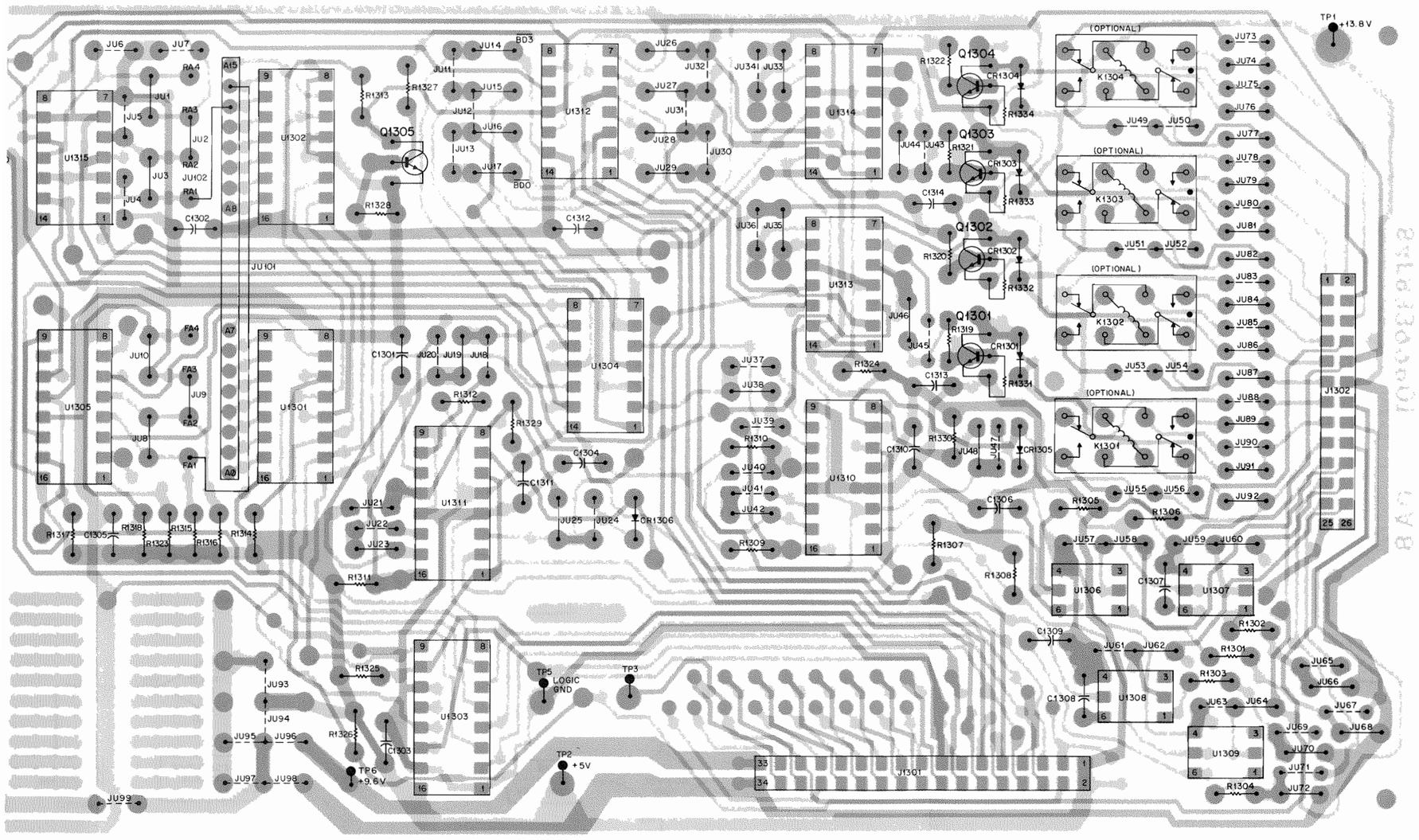


SHOWN FROM COMPONENT SIDE

Notes:

1. Jumpers that are normally installed are shown as heavy lines, optional jumpers are shown with dashed lines.
2. Red dot on relay must be aligned with white dot on PCB during installation.

Circuit Board Detail and Parts List
Motorola No. ***PEPS-37995-C***
(Sheet 1 of 2)
1/7/87- UP



JUMPER DESIGNATION
- NORMALLY IN
- NORMALLY OUT

J1301

+50 VDC	1	2	+5.0 VDC
IPCB	3	4	$\overline{\text{RESET}}$
BA0	5	6	BA1
BA2	7	8	BA3
$\overline{\text{BD0}}$	9	10	$\overline{\text{BD1}}$
$\overline{\text{BD2}}$	11	12	$\overline{\text{BD3}}$
LOGIC GROUND	13	14	$\overline{\text{DATA STROBE}}$
LOGIC GROUND	15	16	DIGITAL (S.P.)
DIGITAL (S.P.)	17	18	DIGITAL (S.P.)
DIGITAL (S.P.)	19	20	AUDIO (S.P.)
AUDIO (S.P.)	21	22	AUDIO (S.P.)
AUDIO (S.P.)	23	24	SELECT AUDIO
LOCAL AUDIO	25	26	TX DATA AUDIO
RX2 AUDIO	27	28	TX AUDIO
AUDIO GROUND	29	30	RX AUDIO
QUAD AUDIO	31	32	AUDIO REFERENCE
+9.6 VDC	33	34	+13.8 VDC

J1302

	K1303 N.O.	1	2	Q1304 OUTPUT
	K1303 WIPER	3	4	K1304 WIPER
	Q1303 OUTPUT	5	6	K1304 N.O.
OUTPUTS	K1302 N.O.	7	8	+5.0 VDC
	K1302 WIPER	9	10	LOGIC GROUND
	Q1302 OUTPUT	11	12	+13.8 VDC
	K1301 N.O.	13	14	AUDIO GROUND
	K1301 WIPER	15	16	I2 (+)
	Q1301 OUTPUT	17	18	I0 (+)
REVERSE WILDCARD INPUTS	I3 (-)	19	20	I0 (-)
	I3 (+)	21	22	I1 (-)
	I1 (+)	23	24	I2 (-)
	SPARE	25	26	NOT USED

OUTPUTS

REVERSE WILDCARD INPUTS

BASE DETAIL

Q1301 – Q1305

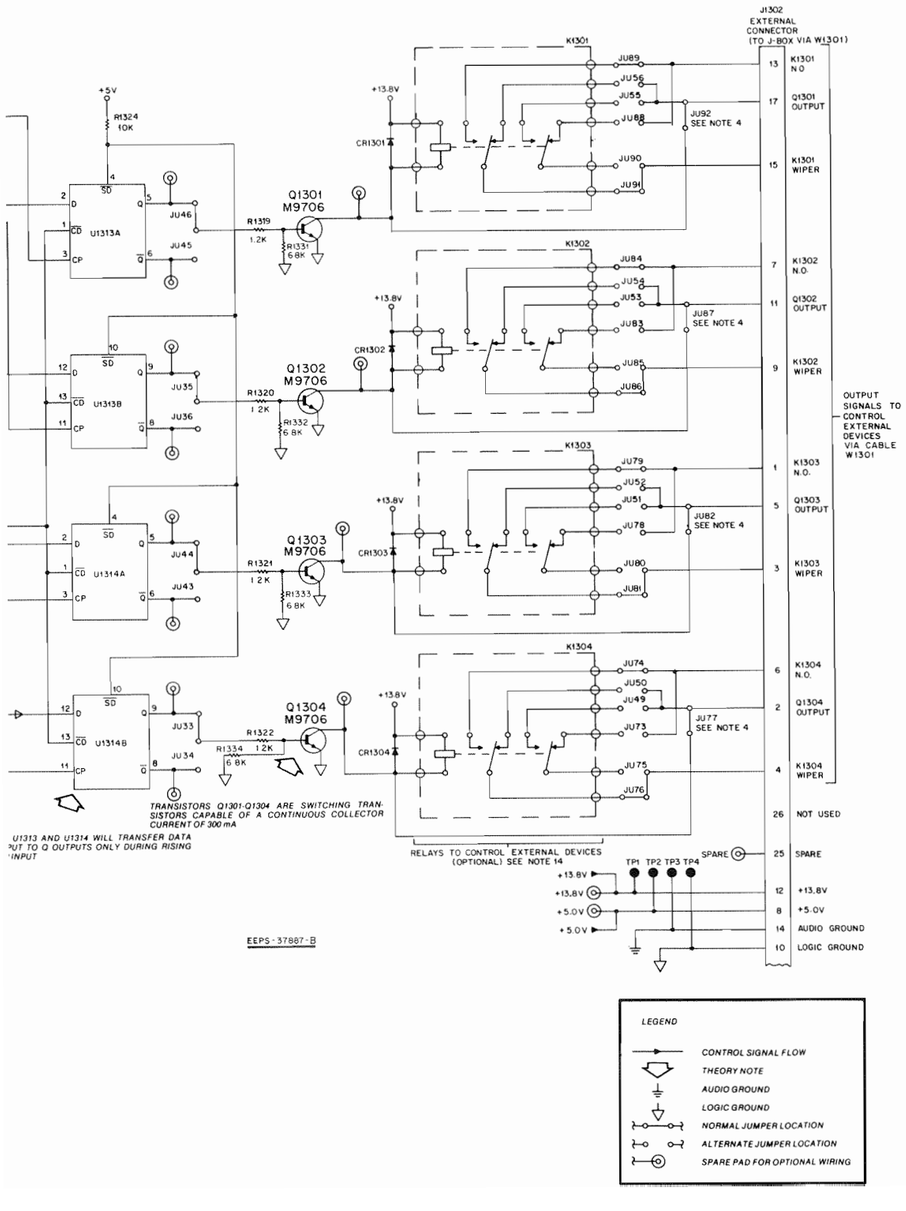
SHOWN FROM COMPONENT SIDE

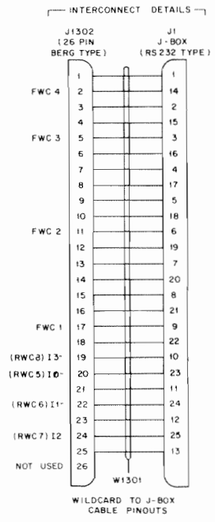
COMPONENT SIDE = BD-EEPS-37903-0
SOLDER SIDE = BD-EEPS-37904-0
OL-EEPS-37905-A

eavy lines, optional jumpers

ᵖCB during installation.

WILDCARD MODULE
MODEL TRN5175A





NOTES:

1. Resistors R1301-R1304 are selected for approximately 22 mA of current to optoisolator U1306-U1309 input(s) based on a control voltage of +10.8 V to +16.3 V DC. Resistors R1301-R1304 should be changed to 1.1k ±5%, 1/4 W, if the control voltage is +24.0 V DC or 220 ohms ±5%; 1/4 W, if the control voltage is +5.0 V DC.

2. Jumpers JU39, 40 and 47 can be installed and jumper JU48 removed when it is desired to have flip flop U1310 cross reset with the other half of flip flop U1310 upon receipt of an external pulse I0 or I1. Jumpers JU20, 21 and 24 are put in and jumper JU25 is removed when it is desired to have flip flop U1311 cross reset with the other half of flip flop U1311 upon receipt of an external pulse I2 or I3.

3. Jumpers JU1-3 and 8-10 can be arranged to allow any address from A0 thru A15 to control any forward wildcard and††or reverse wildcard function.

4. Jumpers JU77, 82, 87 and 92 are used if it is desired to control some external device by the relay driver transistor Q1301-Q1304, when not using the relays, which are optional.

5. Jumpers JU26-29 are normally installed, however, by arranging jumpers JU26 thru JU32, one or any of the data lines can control one or more of the relay drivers.

6. Jumpers JU14-17 are normally installed, however, by arranging jumpers JU11-17 any reverse wildcard input can be gated onto any of the data lines ($\overline{BD0}$-$\overline{BD4}$).

7. Jumper JU101 is used to pass the desired forward wildcard address that will control a forward wildcard function. Jumper JU102 is used to pass the desired reverse wildcard address that will gate any reverse wildcard input onto the data bus. Jumper Ju102 could be used to control a forward wildcard function if desired.

8. Jumpers shown as dashed lines are normally installed.

9. Jumpers JU4-7 are not normally used but are available to ground one or more of the inputs to the reverse wildcard address drivers U1315 when not used.

10. Unless otherwise specified, all resistors values are in ohms, and all capacitor values are in microfarads.

11. Unless otherwise specified, all voltage measurements are dc and and should be made using a DVM with at least 10 megohms††volt input impedance for increased accuracy.

12. Abbreviations:
    FWA — Forward Wildcard Address Line
    RWA — Reverse Wildcard Address Line
    RWD — Reverse Wildcard Data Line

13. Pins 11 and 12 of U1303 are not used.

14. Relays K1301-K1304 are optional and are installed by the user, if required.

15. A 0.01 uFd bypass capacitor is connected between +5.0 V and ground for all IC's except U1306-U1309.

Ic Power Supply Pinouts

IC No.	+5 V	Logic Ground	Bypass Capacitor
1301	16	8	C1301
1302	16	8	C1302
1303	16	8	C1303
1304	14	7	C1304
1305	16	8	C1305
1306	—	4	—
1307	—	4	—
1308	—	4	—
1309	—	4	—
1310	5	13	C1310
1311	5	13	C1311
1312	14	7	C1312
1313	14	7	C1313
1314	14	7	C1314
1315	14	7	C1315

Jumper No.	Function
*1, 2, 3	Selects which reverse wildcard address drivers are activated by the reverse wildcard address.
4, 5, 6, 7	Used to ground input to an address driver if the address driver (U1315A-D) is not used.
*8, 9, 10	Selects which forward wildcard address drivers are activated by the forward wildcard address.
11, 12, 13	Used to allow any reversed wildcard input (RWD1-RDW4) to be gated onto any of the data lines.
*14, 15, 16, 17	Connects the data bus control gate output to the data line.
18, 22, 37, 41	Used to connect the $\overline{Q}$ output of flip flops U1310 and U1311 to the data bus control gates U1304.
*19, 23, 38, 42	Connects the Q output of flip flops U1310 and U1311 to the data bus control gates U1304.
20, 21, 24	Use to cross reset flip flop U1311. Jumper JU25 must be removed during cross reset.
*25	Allows both halves of flip flop U1311 to come out of RESET as being RESET.
*26, 27, 28, 29	Connects the data bus pulses (BD0-BD3) to the relay driver flip flops U1313 and U1314.
30, 31, 32	Used to allow one of the four data lines to control one or all four relay driver circuits. Used in association with jumpers JU26 thru JU29.
*33, 35, 44, 46	Connects the Q output of flip flops U1313-U1314 to the applicable relay driver Q1301-Q1304. This allows a logic 1 at Q to active the transistor and relay.
34, 36, 43, 45	Used if the $\overline{Q}$ output of flip flops U1313-U1314 are required.
39, 40, 47	Use to cross reset flip flop U1310. Jumper JU48 must be removed during cross reset.
*48	Allows both halves of flip flop U1310 to come out of RESET as being RESET.
49 thru 56	Used if the normally closed contacts of relays K1301-K1304 are required to operated external devices.
57, 59, 61, 63	Used to supply the ground path if the external device signal is the power source for reverse wildcard inputs.
*58, 60, 62, 64	Provides a ground path from opto isolator U1306-U1309 that can be switched by the external device to generate reverse wildcard function inputs.
65, 67, 69, 71	Used when the external device supplies power as it's input signal.
*66, 68, 70, 72	Provides power to the opto isolator U1306-U1309 when the external device switches the ground path to generate reverse wildcard function inputs.
73, 78, 83, 88	Used if the normally open contacts of relays K1301-K1304 are required to operate external devices.
*74, 79, 84, 89	Connects normally open contacts of relays K1301-K1304 to external devices.
75, 80, 85, 90	Used to connect relay wiper contacts to the external device.
*76, 81, 86, 91	Connects wiper contacts of relays K1301-K1304 to the external device.
*77, 82, 87, 92	Provides an output signal that is controlled directly by transistor Q1301-Q1304.
92 thru 100	Provides A+, +9.6 V and +5 V to custom circuit area.
*101	Used to connect the active low A14 output from address decoder U1302 to the wildcard address driver U1305. Any decoder output can be selected by use of this jumper but address A14 is usually used to match the diagnostic metering panel bit display.
*102	Used to connect the active low A13 output from address decoder U1302 to the wildcard address driver U1305. Any decoder output can be selected by used of this jumper but address A13 is usually used to match the diagnostic metering panel bit display.

*indicates jumpes that are normally in.

Schematic Diagram
Motorola No. PEPS-37995-C
(Sheet 2 of 2)
1/7/87- UP

— REVERSE WILDCARD FUNCTION —

REVERSE WILDCARD INPUTS (FROM EXTERNAL DEVICES)

J1302 EXTERNAL CONNECTOR (FROM J-BOX)

I0(+) 18 — JU67 — R1301 620 (SEE NOTE 1) — JU68 — +13.8V — OPTO ISOLATOR U1306 — C1306 .0068
I0(-) 20 — JU58 — JU57
I1(+) 23 — JU65 — R1302 620 (SEE NOTE 1) — JU66 — +13.8V — OPTO ISOLATOR U1307 — C1307 .0068
I1(-) 22 — JU60 — JU59
I2(+) 16 — JU69 — R1303 620 (SEE NOTE 1) — JU70 — +13.8V — OPTO ISOLATOR U1308 — C1308 .0068
I2(-) 24 — JU62 — JU61
I3(+) 21 — JU71 — R1304 620 (SEE NOTE 1) — JU72 — +13.8V — OPTO ISOLATOR U1309 — C1309 .0068
I3(-) 19 — JU64 — JU63

STANDARD JUMPERING ALLOWS A REVERSE WILDCARD INPUT TO BE GENERATED WHEN THE EXTERNAL DEVICE PROVIDES A GROUND PATH VIA PINS 20, 22, 24, OR 19

RESISTORS R1301-R1304 SHOULD BE SELECTED TO PROVIDE 20 mA THROUGH OPTO ISOLATOR (U1306-U1309) WHEN ACTIVE

U1310A INPUT PULSE LATCH: R1309 10K, R1305 10K, +5V, SD, K, CD, Q, CP, J; RWD 1, $\overline{RWD\ 1}$; JU42, JU41, JU39, JU40, SEE NOTE 2

U1310B INPUT PULSE LATCH: R1310 10K, R1330 10K, R1306 10K, CR1305, JU47, JU48; RWD 2, $\overline{RWD\ 2}$; JU38, JU37

U1311A INPUT PULSE LATCH: R1311 10K, R1307 10K; RWD 3, $\overline{RWD\ 3}$; JU23, JU22, JU20, JU21, SEE NOTE 2

U1311B INPUT PULSE LATCH: R1312 10K, R1329 10K, R1308 10K, CR1306, JU24, JU25; RWD 4, $\overline{RWD\ 4}$; JU19, JU18

DATA STROBE

CLEAR DATA

INPUT FROM MUXBUS

J1301: DATA STROBE (14), +5V (2), +5V (1), RESET (4), +13.8V (34), +9.6V (33), TX DATA AUDIO (26), RX 2 AUDIO (27), TX AUDIO (28), RX AUDIO (30), INPUT ADDRESS BA2 (7), BA1 (6), BA0 (5), QUAD AUDIO (31), SELECT AUDIO (24), LOCAL AUDIO (25), IPCB (3), INPUT ADDRESS BA3 (8), DIGITAL (S P) (16, 17, 18, 19), AUDIO (S P) (20, 21, 22, 23), AUDIO GROUND (29), AUDIO REFERENCE (32), LOGIC GROUND (15), LOGIC GROUND (13), INPUT DATA $\overline{BD3}$ (12), $\overline{BD2}$ (11), $\overline{BD1}$ (10), $\overline{BD0}$ (9)

+13.8V, +9.6V, TP6, TP5

Q1305 TURNS ON WITH RESET BIT FROM MUXBUS

Q1305 M9706; R1313 1K; R1326 47K; U1312D; R1327 2.7K; R1328 10K; R1325 47K; U1303E

NON-INVERTING BUFFERS: U1303D, U1303C, U1303B

U1301 1-8 ADDRESS DECODER: R1314 10K, E3, A0, A1, A2, $\overline{E2}$, $\overline{E1}$, $\overline{Q0}$–$\overline{Q7}$, A8–A15; U1303A

U1302 1-8 ADDRESS DECODER: E3, A0, A1, A2, $\overline{E2}$, $\overline{E1}$, $\overline{Q0}$–$\overline{Q7}$, A8–A15

JU102 SEE NOTE 7

U1312E

INHIBITS WRITING A BIT ON DATA BUS DURING RESET

NC — S1301 — OPERATE / RESET

DISABLES ALL SIGNALS FROM EXTERNAL DEVICES WHEN IN RESET

JU8 SEE NOTE 3; JU9 SEE NOTE 3; JU10 SEE NOTE 3; JU101 SEE NOTE 7

U1305 WILDCARD ADDRESS DRIVERS: R1323 10K, $\overline{MR}$, DO, D1, D2, D3, CP, $\overline{Q0}$–$\overline{Q3}$, Q0–Q3; FWA 1 (R1315 47K), FWA 2 (R1316 47K), FWA 3 (R1317 47K), FWA 4 (R1318 47K), +5V

DATA BUS ($\overline{BD0}$ THRU $\overline{BD3}$) CARRIES DATA FROM THE MUX BUS DURING FORWARD WILDCARD OPERATION TO CONTROL AN EXTERNAL DEVICE OR WILL CARRY A BIT TO THE MUXBUS THAT REPRESENTS A SIGNAL FROM AN EXTERNAL DEVICE DURING REVERSE WILDCARD OPERATION

CLEAR DATA SIGNAL WILL RESET TRANSISTOR DRIVERS U1313 AND U1314

CLEAR DATA

REVERSE WILDCARD ADDRESS DRIVERS: RWA1, RWA 2, RWA 3, RWA 4; U1315A, U1315B, U1315C, U1315D; JU3 SEE NOTE 3, JU4 SEE NOTE 9, JU2 SEE NOTE 3, JU5 SEE NOTE 9, JU1 SEE NOTE 3, JU6 SEE NOTE 9, JU7 SEE NOTE 9

U1304B, U1304A, U1304D, U1304C; JU17 SEE NOTE 6, JU13, JU16, JU12, JU15, JU11, JU14

DATA BUS CONTROL GATES (U1304) WILL WRITE A BIT ON DATA BUS WHEN THE OUTPUT(S) IS LOW. U1304 OUTPUTS ARE OPEN COLLECTOR

BUS BUFFERS: U1312A, U1312B, U1312C, U1312F; JU29 SEE NOTE 5, JU30, JU28, JU31, JU27, JU32, JU26

FLIP FLOPS U1313 AND U1314 FROM D INPUT TO Q OUTPUTS EDGE OF CP INPUT.

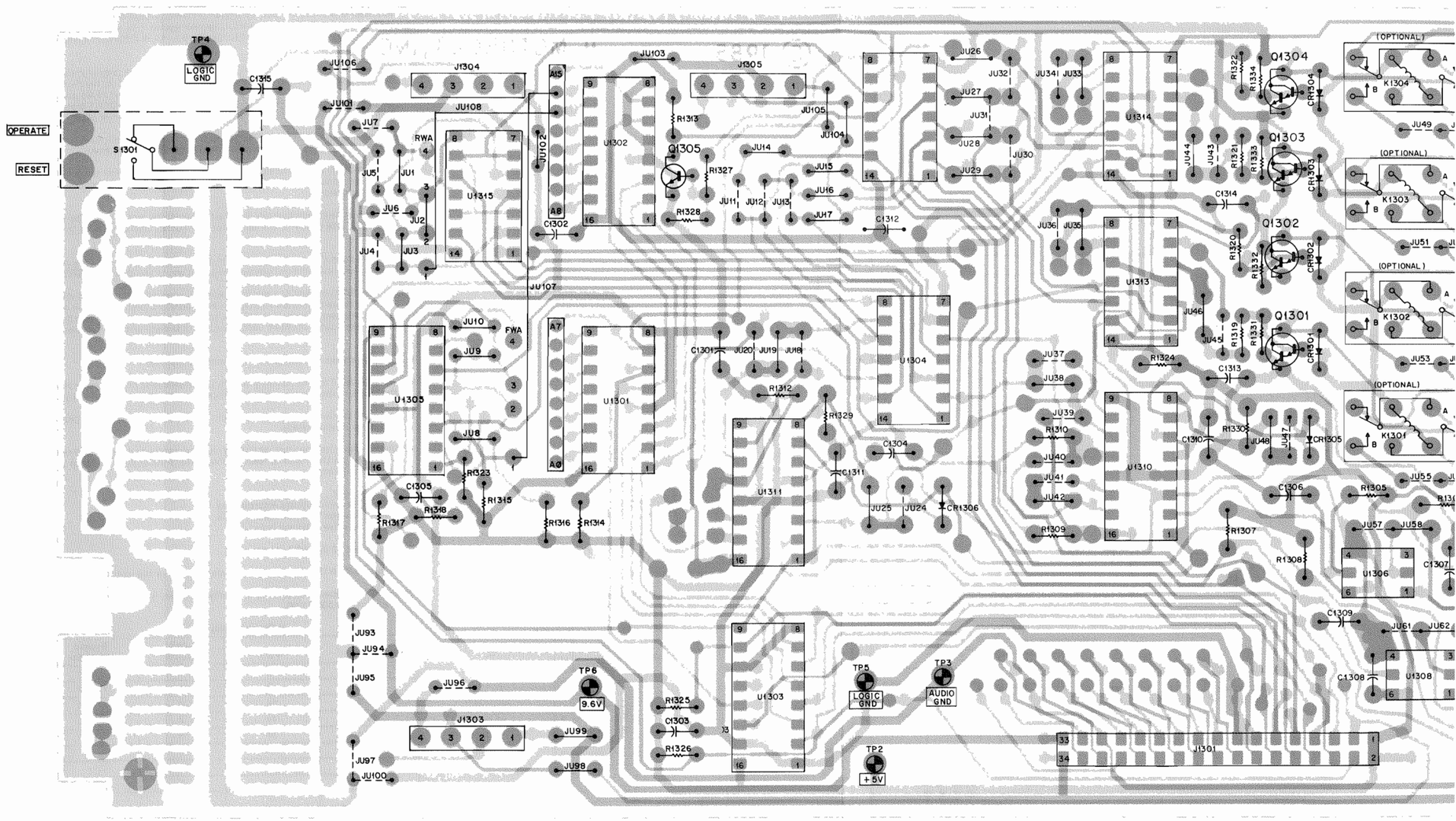
WILDCARD MODULE
MODEL TRN9754A

parts list

TRN9754A Wildcard Board — PL-9633-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed:
C1301 thru 1305	21-11021G07	.01 uF +100-0%; 50 V
C1306 thru 1309	8-11017B07	.0068 uF ±10%; 100 V
C1310 thru 1315	21-11021G07	.01 uF +100-0%; 50 V
		diode: (see note)
CR1305, 1306	48-11034D01	silicon
		connector, receptacle:
J1301	28-83136N05	male; 34-contact
J1302	28-83136N01	male; 26-contact
J1303 thru 1305	28-83447L14	male; 4-contact
		transistor: (see note)
Q1301 thru 1305	48-869706	NPN; type M9706
		resistor, fixed: ±5%; 1/4 W: unless otherwise stated
R1301 thru 1304	6-11009E44	620
R1305 thru 1312	6-11009E73	10k
R1313	6-11009E49	1k
R1314	6-11009E73	10k
R1315 thru 1318	6-11009E89	47k
R1319 thru 1322	6-11009E51	1.2k
R1323, 1324	6-11009E73	10k
R1325, 1326	6-11009E89	47k
R1327	6-11009E59	2.7k
R1328	6-11009E73	10k
R1329, 1330	6-11009E89	47k
R1331 thru 1334	6-11009E69	6.8k
		switch:
S1301	40-83685N12	spdt
		integrated circuit: (see note)
U1301, 1302	51-84561L41	binary address decoder
U1303	51-84561L77	hex tri-state buffer
U1304	51-84371K83	quad NAND gate
U1305	51-82609M73	quad D-type flip-flop
U1306 thru 1309	51-83629M75	opto-isolator
U1310, 1311	51-84561L88	dual JK flip-flop
U1312	51-84561L03	hex inverter
U1313, 1314	51-84561L34	dual D-type flip-fllop
U1315	51-84561L06	quad 2-input NOR gate
		mechanical parts
	6-11009F23	JUMPER, zero ohm resistor; 52 used
	29-10271A15	PIN, test; 6 used (TP1 thru 6)

note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.



SHOWN FROM COMPONENT SIDE

COMPONENT SIDE : BD-EEPS-41739-O
SOLDER SIDE : BD-EEPS-41740-O
OL-EEPS-41741-O

Circuit Board Detail and Parts List
Motorola No. ***PEPS-41709-A***
(Sheet 1 of 2)
1/7/87- UP

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PL-9633-A

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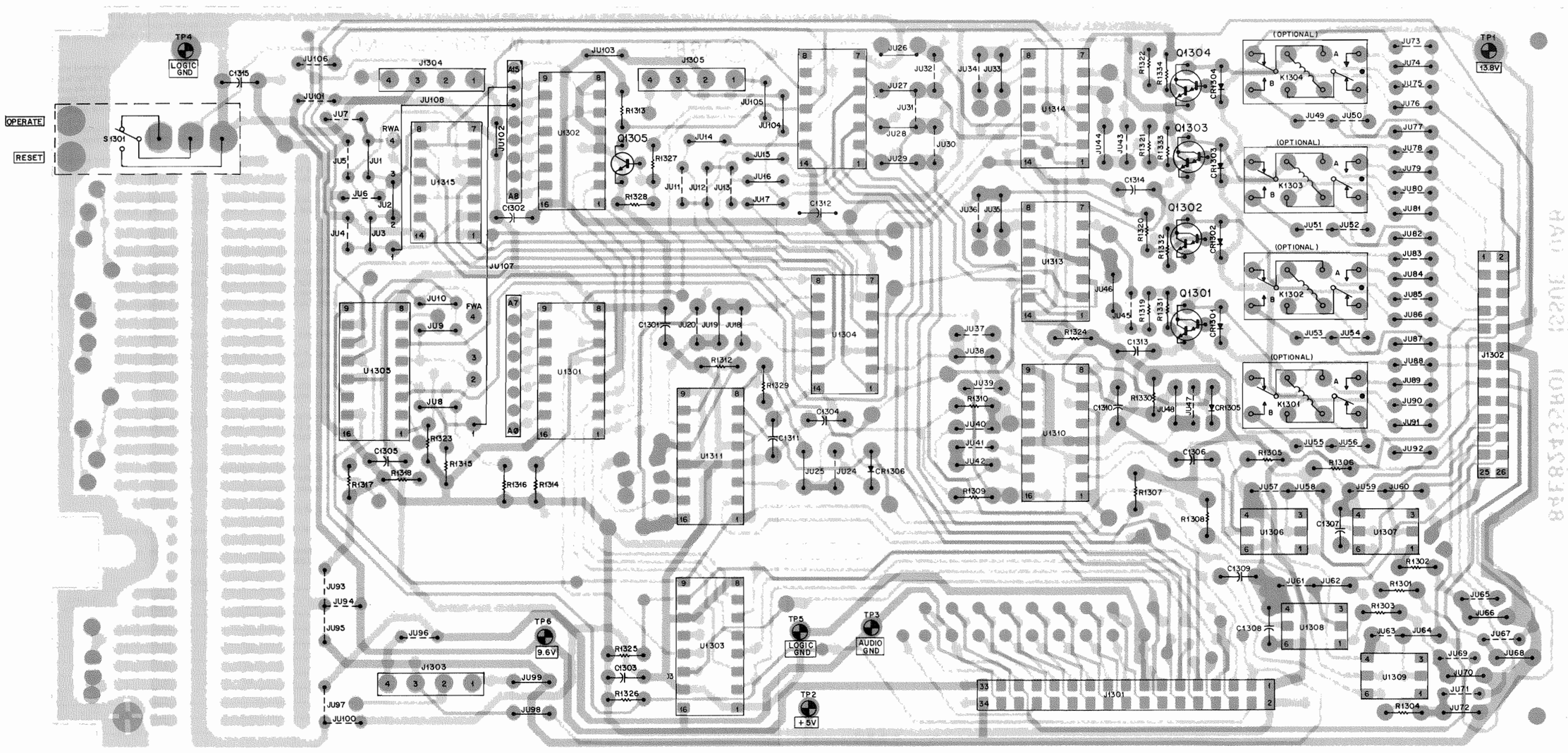
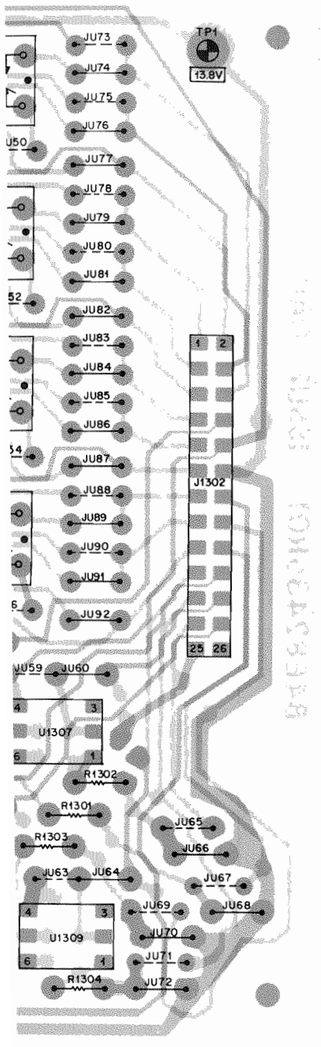
stor; 52 used
ıru 6)

ırated circuits must



SHOWN FROM COMPONENT SIDE

COMPONENT SIDE : BD-EEPS-41739-0
SOLDER SIDE : BD-EEPS-41740-0
OL-EEPS-41741-0



JUMPER DESIGNATION

●——● NORMALLY IN

●- - -● NORMALLY OUT

J1301

+5.0 VDC	1	2	+5.0 VDC
IPCB	3	4	$\overline{\text{RESET}}$
BA0	5	6	BA1
BA2	7	8	BA3
$\overline{\text{BD0}}$	9	10	$\overline{\text{BD1}}$
$\overline{\text{BD2}}$	11	12	$\overline{\text{BD3}}$
LOGIC GROUND	13	14	$\overline{\text{DATA STROBE}}$
LOGIC GROUND	15	16	DIGITAL (S.P.)
DIGITAL (S.P.)	17	18	DIGITAL (S.P.)
DIGITAL (S.P.)	19	20	AUDIO (S.P.)
AUDIO (S.P.)	21	22	AUDIO (S.P.)
AUDIO (S.P.)	23	24	SELECT AUDIO
LOCAL AUDIO	25	26	TX DATA AUDIO
RX2 AUDIO	27	28	TX AUDIO
AUDIO GROUND	29	30	RX AUDIO
QUAD AUDIO	31	32	AUDIO REFERENCE
+9.6 VDC	33	34	+13.8 VDC

J1302

	K1303 N.O.	1	2	Q1304 OUTPUT
	K1303 WIPER	3	4	K1304 WIPER — OUTPUTS
	Q1303 OUTPUT	5	6	K1304 N.O.
OUTPUTS —	K1302 N.O.	7	8	+5.0 VDC
	K1302 WIPER	9	10	LOGIC GROUND
	Q1302 OUTPUT	11	12	+13.8 VDC
	K1301 N.O.	13	14	AUDIO GROUND
	K1301 WIPER	15	16	2 (+)
	Q1301 OUTPUT	17	18	0 (+) — REVERSE WILDCARD INPUTS
REVERSE WILDCARD INPUTS —	3 (-)	19	20	0 (-)
	3 (+)	21	22	1 (-)
	1 (+)	23	24	2 (-)
	SPARE	25	26	NOT USED

BASE DETAIL

Q1301 – Q1305

J1303

1	+13.8V
2	SPARE
3	IPCB
4	SPARE

J1304

1	LOGIC GND
2	$\overline{\text{RESET}}$
3	+9.6V
4	SPARE

J1305

1	$\overline{\text{A7}}$
2	+5V
3	$\overline{\text{BD0}}$
4	SPARE

NOTES:

1. Resistors R1301-R1304 are selected for approximately 22 mA of current to opto isolator U1306-U1309 input(s) based on a control voltage of +10.8 V to +16.3 V DC. Resistors R1301-R1304 should be changed to 1.1k ±5%, 1/4 W, if the control voltage is +24 V DC, or 220 ohms ±5%; 1/4 W, if the control voltage is +5 V DC.

2. Jumpers JU39, 40 and 47 can be installed and jumper JU48 removed when it is desired to have flip-flop U1310 cross-reset with the other half of flip-flop U1310 upon receipt of an external pulse at input 0 or 1. Jumpers JU20, 21 and 24 are put in and jumper JU25 is removed when it is desired to have flip-flop U1311 cross-reset with the other half of flip-flop U1311 upon receipt of an external pulse at input 2 or 3.

3. Jumpers JU1-3 and 8-10 can be arranged to allow any address from A0 thru A15 to control any forward wildcard and/or reverse wildcard function.

4. Jumpers JU77, 82, 87 and 92 are used if it is desired to control some external device by the relay driver transistor Q1301-Q1304, when not using the relays, which are optional.

5. Jumpers JU26 thru 29 are normally installed, however, by arranging jumpers JU26 thru JU32, one or any of the data lines can control one or more of the relay drivers.

6. Jumpers JU14 thru 17 are normally installed, however, by arranging jumpers JU11 thru 17 any reverse wildcard input can be gated onto any of the data lines ($\overline{\text{BD0}}$-$\overline{\text{BD4}}$).

7. Jumper JU107 is used to pass the desired forward wildcard address that will control a forward wildcard function. Jumper JU108 is used to pass the desired reverse wildcard address that will gate any reverse wildcard input onto the data bus.

8. Jumpers shown as solid lines are normally installed.

9. Jumpers JU4-7 are not normally used but are available to disable one or more of the inputs of the reverse wildcard address drivers U1315 when not used.

10. Unless otherwise specified, all resistors values are in ohms, and all capacitor values are in microfarads.

11. Unless otherwise specified, all voltage measurements are dc and and should be made using a DVM with at least 10 Megohms/Volt input impedance for increased accuracy.

12. Abbreviations:
    FD — Forward Data
    FWA — Forward Wildcard Address
    FWC — Forward Wildcard Control
    RWA — Reverse Wildcard Address
    RWD — Reverse Wildcard Data
    RW — Reverse Wildcard

13. Pins 11 and 12 of U1303 are not used.

14. Relays K1301-K1304 and diodes CR1301-CR1304 are optional and are installed by the user, as desired.

15. A 0.01 uFd bypass capacitor is connected between +5 V and ground for all IC's except U1306-U1309.

IC Power Supply Pinouts

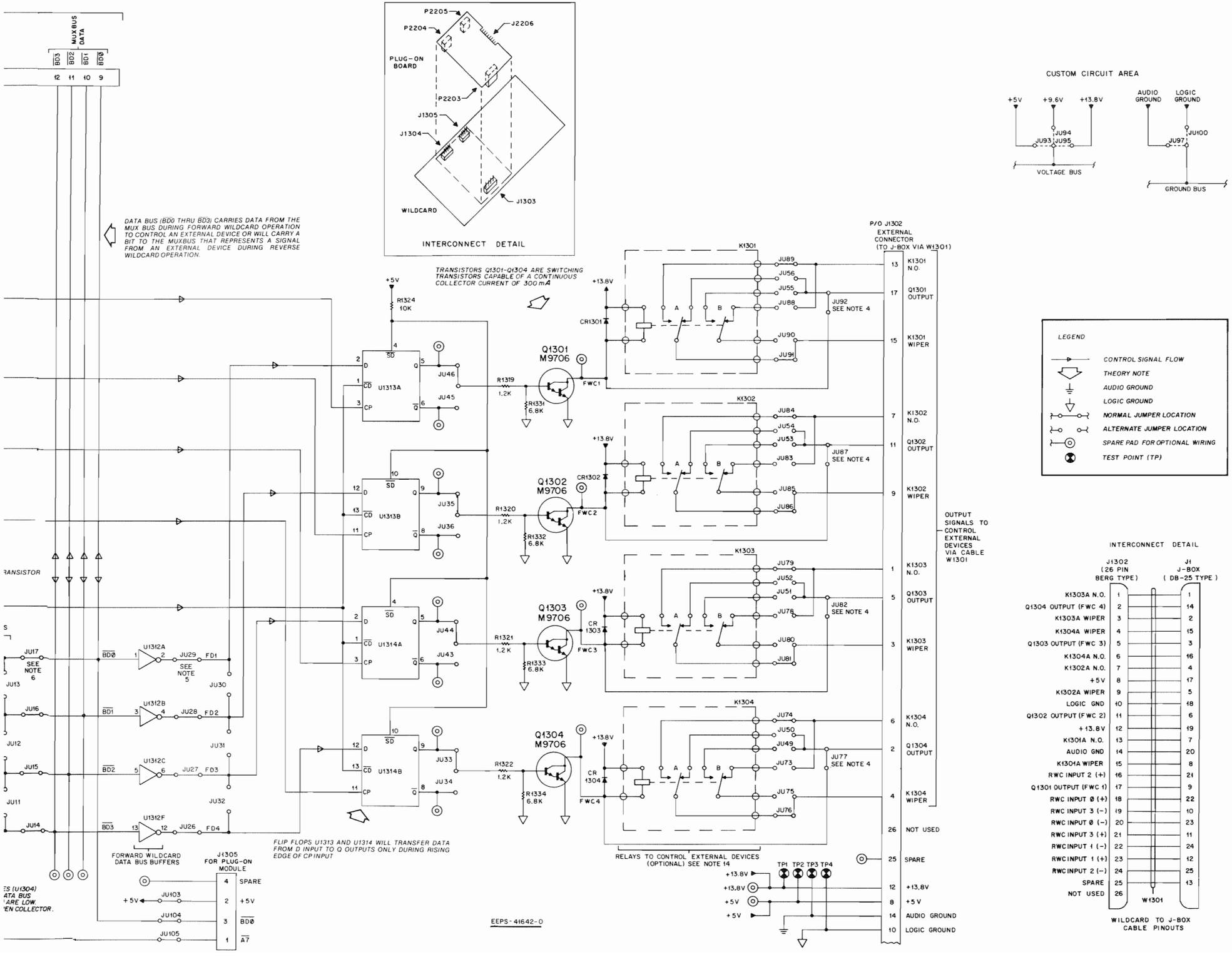
IC No.	+5 V	Logic Ground	Bypass Capacitor
1301	16	8	C1301
1302	16	8	C1302
1303	16	8	C1303
1304	14	7	C1304
1305	16	8	C1305
1306	—	4	—
1307	—	4	—
1308	—	4	—
1309	—	4	—
1310	5	13	C1310
1311	5	13	C1311
1312	14	7	C1312
1313	14	7	C1313
1314	14	7	C1314
1315	14	7	C1315

Jumper Table

Jumper No.	Function
*1, 2, 3	Selects which reverse wildcard address drivers are activated by the reverse wildcard address.
4, 5, 6, 7	Used to disable input to an address driver if the address driver (U1315A-D) is not used.
*8, 9, 10	Selects which forward wildcard address drivers are activated by the forward wildcard address.
11, 12, 13	Used to allow any reversed wildcard input (RWD1-RDW4) to be gated onto any of the data lines.
*14, 15, 16, 17	Connects the data bus control gate output to the data line.
18, 22, 37, 41	Used to connect the $\overline{\text{Q}}$ output of flip flops U1310 and U1311 to the data bus control gates U1304.
*19, 23, 38, 42	Connects the Q output of flip flops U1310 and U1311 to the data bus control gates U1304.
20, 21, 24	Use to cross reset flip flop U1311. Jumper JU25 must be removed during cross reset.
*25	Allows both halves of flip flop U1311 to come out of RESET as being RESET.
*26, 27, 28, 29	Connects the data bus pulses (BD0-BD3) to the relay driver flip flops U1313 and U1314.
30, 31, 32	Used to allow one of the four data lines to control one or all four relay driver circuits. Used in association with jumpers JU26 thru JU29.
*33, 35, 44, 46	Connects the Q output of flip flops U1313-U1314 to the applicable relay driver Q1301-Q1304. This allows a logic 1 at Q to active the transistor and relay.
34, 36, 43, 45	Used if the $\overline{\text{Q}}$ output of flip flops U1313-U1314 are required.
39, 40, 47	Use to cross reset flip flop U1310. Jumper JU48 must be removed during cross reset.
*48	Allows both halves of flip-flop U1310 to come out of RESET as being RESET.
49 thru 56	Used if the normally closed contacts of relays K1301-K1304 are required to operated external devices.
57, 59, 61, 63	Used to supply the ground path if the external device signal is the power source for reverse wildcard inputs.
*58, 60, 62, 64	Provides a ground path from opto isolator U1306-U1309 that can be switched by the external device to generate reverse wildcard function inputs.
65, 67, 69, 71	Used when the external device supplies power as it's input signal.
*66, 68, 70, 72	Provides power to the opto isolator U1306-U1309 when the external device switches the ground path to generate reverse wildcard function inputs.
73, 78, 83, 88	Used if the normally open contacts of relays K1301-K1304 are required to operate external devices.
*74, 79, 84, 89	Connects normally open contacts of relays K1301-K1304 to external devices.
75, 80, 85, 90	Used to connect relay wiper contacts to the external device.
*76, 81, 86, 91	Connects wiper contacts of relays K1301-K1304 to the external device.
*77, 82, 87, 92	Provides an output signal that is controlled directly by transistor Q1301-Q1304.
93,94,95	Provides either +5 V, +9.6 V or +13.8 V, respectively, to the custom circuit area of the wildcard module.
96	Provides an audio ground path for the plug-on board.
97	Provides an audio ground path to the custom circuit area.
*98	Allows the plug-on board to have access to the Expansion Bus IPCB line.
*99	Provides 13.8 V (A+) for the plug-on board.
100	Provides a logic ground to the custom circuit area.
*101	Provides +9.6 V for the plug-on board.
*102	Provides a logic ground for the plug-on board.
*103	Provides +5 V for the plug-on board.
*104	Allows the plug-on board to have access to the MUXbus $\overline{\text{BD0}}$ line.
*105	Allows the plug-on board to have access to one of the wildcard decoded MUXbus addresses, typically address $\overline{\text{A7}}$ is used.
*106	Used to route $\overline{\text{RESET}}$ to the plug-on board.
*107	Used to connect the active low A14 output from address decoder U1302 to the wildcard address driver U1305. Any decoder output can be selected by use of this jumper but address A14 is usually used to match the diagnostic metering panel bit display.
*108	Used to connect the active low A13 output from address decoder U1302 to the wildcard address driver U1305. Any decoder output can be selected by used of this jumper but address A13 is usually used to match the diagnostic metering panel bit display.

* Indicates jumpers that are normally in.

WILDCARD MODULE
MODEL TRN9754A



INTERCONNECT DETAIL

	J1302 (26 PIN BERG TYPE)	J1 J-BOX (DB-25 TYPE)
K1303A N.O.	1	1
Q1304 OUTPUT (FWC 4)	2	14
K1303A WIPER	3	2
K1304A WIPER	4	15
Q1303 OUTPUT (FWC 3)	5	3
K1304A N.O.	6	16
K1302A N.O.	7	4
+5V	8	17
K1302A WIPER	9	5
LOGIC GND	10	18
Q1302 OUTPUT (FWC 2)	11	6
+13.8V	12	19
K1301A N.O.	13	7
AUDIO GND	14	20
K1301A WIPER	15	8
RWC INPUT 2 (+)	16	21
Q1301 OUTPUT (FWC 1)	17	9
RWC INPUT Ø (+)	18	22
RWC INPUT 3 (-)	19	10
RWC INPUT Ø (-)	20	23
RWC INPUT 3 (+)	21	11
RWC INPUT 1 (-)	22	24
RWC INPUT 1 (+)	23	12
RWC INPUT 2 (-)	24	25
SPARE	25	13
NOT USED	26	

W1301

WILDCARD TO J-BOX CABLE PINOUTS

Schematic Diagram
Motorola No. PEPS-41709-A
(Sheet 2 of 2)
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J1301 I/O VIA OPTIONS CABLE

+9.6V (33) · LOGIC GND (15) · LOGIC GND (13) · AUDIO GND (29) · IPCB (3) · DATA STROBE (14) · +5V (2) · +5V (1) · RESET (4) · +13.8V (34) · TX DATA AUDIO (26) · RX 2 AUDIO (27) · TX AUDIO (28) · RX AUDIO (30) · BA3 (8) · BA2 MUXBUS ADDRESS (7) · BA1 (6) · BA0 (5) · QUAD AUDIO (31) · SELECT AUDIO (24) · LOCAL AUDIO (25) · SPARE DIGITAL I/O (16, 17, 18, 19) · SPARE AUDIO I/O (20, 21, 22, 23) · AUDIO REFERENCE (32) · MUXBUS DATA BD3 (12) · BD2 (11) · BD1 (10) · BD0 (9)

TP6 · TP5 · +13.8V

:SE WILDCARD
DATA LATCHES

U1310A INPUT PULSE LATCH — R1309 10K — RWD 1 — JU42 — JU41 — RWD 1 — JU39 — SEE NOTE 2 — JU40

U1310B INPUT PULSE LATCH — R1310 10K — RWD 2 — JU38 — JU37 — RWD 2

U1311A INPUT PULSE LATCH — R1311 10K — RWD 3 — JU23 — JU22 — RWD 3 — JU20 — SEE NOTE 2 — JU21

U1311B INPUT PULSE LATCH — R1312 10K — RWD 4 — JU19 — JU18 — RWD 4

Q1305 TURNS ON WITH RESET BIT FROM MUXBUS

Q1305 M9706 — +5V — R1313 1 K — U1312D — R1327 2.7K — R1326 47 K — R1328 10K — +5V — +5V — R1325 47K — U1303E

NON-INVERTING BUFFERS — U1303D — U1303C — U1303B — U1303A

U1301 1-8 ADDRESS DECODER — +5V — R1314 10K — E3 — A0 A1 A2 — $\overline{E2}$ $\overline{E1}$ — $\overline{Q0}$ $\overline{Q1}$ $\overline{Q2}$ $\overline{Q3}$ $\overline{Q4}$ $\overline{Q5}$ $\overline{Q6}$ $\overline{Q7}$ — $\overline{A0}$ $\overline{A1}$ $\overline{A2}$ $\overline{A3}$ $\overline{A4}$ $\overline{A5}$ $\overline{A6}$ $\overline{A7}$

U1302 1-8 ADDRESS DECODER — E3 — A0 A1 A2 — $\overline{E2}$ $\overline{E1}$ — $\overline{Q0}$ $\overline{Q1}$ $\overline{Q2}$ $\overline{Q3}$ $\overline{Q4}$ $\overline{Q5}$ $\overline{Q6}$ $\overline{Q7}$ — $\overline{A8}$ $\overline{A9}$ $\overline{A10}$ $\overline{A11}$ $\overline{A12}$ $\overline{A13}$ $\overline{A14}$ $\overline{A15}$

JU108 SEE NOTE 7

U1305 WILDCARD ADDRESS DRIVERS — +5V — R1323 10K — MR — DO D1 D2 D3 CP — FWA 1 — R1315 47K — JU8 SEE NOTE 3 — FWA 2 — R1316 47K — JU107 SEE NOTE 7 — JU9 SEE NOTE 3 — FWA 3 — R1317 47K — JU10 SEE NOTE 3 — FWA 4 — R1318 47K — +5V — $\overline{Q0}$ Q0 $\overline{Q1}$ Q1 $\overline{Q2}$ Q2 $\overline{Q3}$ Q3

$\overline{CLEAR\ DATA}$ SIGNAL WILL RESET TRANSISTOR DRIVERS U1313 AND U1314.

$\overline{CLEAR\ DATA}$

U1312E

INHIBITS WRITING A BIT ON DATA BUS DURING RESET

NC · OPERATE · RESET · S1301

DISABLES ALL SIGNALS FROM EXTERNAL DEVICES WHEN IN RESET.

DATA STROBE

REVERSE WILDCARD DATA BUS CONTROL GATES

U1315A RWA1 — U1315B RWA 2 — U1315C RWA 3 — U1315D RWA 4 — JU3 SEE NOTE 3 — JU4 SEE NOTE 9 — JU2 SEE NOTE 3 — JU5 SEE NOTE 9 — JU1 SEE NOTE 3 — JU6 SEE NOTE 9 — JU7 SEE NOTE 9 — +5V

REVERSE WILDCARD ADDRESS DRIVERS

U1304B RWD1 — U1304A RWD2 — U1304D RWD3 — U1304C RWD4 — JU17 SEE NOTE 6 — JU13 — JU16 — JU12 — JU15 — JU11 — JU14

DATA BUS CONTROL GATES (U1304) WILL WRITE A BIT ON DATA BUS WHEN THEIR OUTPUT(S) ARE LOW. U1304 OUTPUTS ARE OPEN COLLECTOR.

DATA BUS ($\overline{BD0}$ THRU $\overline{BD3}$) CARRIES DATA FROM THE MUX BUS DURING FORWARD WILDCARD OPERATION TO CONTROL AN EXTERNAL DEVICE OR WILL CARRY A BIT TO THE MUXBUS THAT REPRESENTS A SIGNAL FROM AN EXTERNAL DEVICE DURING REVERSE WILDCARD OPERATION.

FORWARD WILDCARD DATA BUS BUFFERS

U1312A $\overline{BD0}$ — JU29 SEE NOTE 5 — FD1 — JU30 — U1312B $\overline{BD1}$ — JU28 — FD2 — JU31 — U1312C $\overline{BD2}$ — JU27 — FD3 — JU32 — U1312F $\overline{BD3}$ — JU26 — FD4

J1305 FOR PLUG-ON MODULE

4 SPARE · 2 +5V (JU103) · 3 $\overline{BD0}$ (JU104) · 1 $\overline{A7}$ (JU105)

P2205 · P2204 · P2203 · J1305 · J1304 · PLUG-ON BOARD · WILDCARD

INTERCONNECT DETAIL

TRANSISTORS Q1301-Q130
TRANSISTORS CAPABLE OF
COLLECTOR CURRENT OF

+5V — R1324 10K

U1313A — JU46 — JU45 — R1319 1.2K

U1313B — JU35 — JU36 — R1320 1.2K

U1314A — JU44 — JU43 — R1321 1.2 K

U1314B — JU33 — JU34 — R1322 1.2K

FLIP FLOPS U1313 AND U1314 WILL TRANSFER DATA FROM D INPUT TO Q OUTPUTS ONLY DURING RISING EDGE OF CP INPUT.

J1301 I/O VIA OPTIONS CABLE

J1304 FOR PLUG-ON MODULE
SPARE 4 — JU101
+9.6 V 3 — JU102
LOGIC GND 1
RESET 2 — JU106

J1303 FOR PLUG-ON MODULE
SPARE 2
SPARE 4 — JU96 — AUDIO GND
IPCB 3 — JU98
+13.8V 1 — JU99

+9.6V — TP6
TP5

+9.6V 33 | LOGIC GND 15 | LOGIC GND 13 | AUDIO GND 29 | IPCB 3 | DATA STROBE 14 | +5V 2 | +5V 1 | RESET 4 | +13.8V 34 | TX DATA AUDIO 26 | RX 2 AUDIO 27 | TX AUDIO 28 | RX AUDIO 30 | BA3 8 | BA2 7 | BA1 6 | BA0 5 | MUXBUS ADDRESS | QUAD AUDIO 31 | SELECT AUDIO 24 | LOCAL AUDIO 25 | SPARE DIGITAL I/O 16 17 18 19 | SPARE AUDIO I/O 20 21 22 23 | AUDIO REFERENCE 32

REVERSE WILDCARD INPUT DATA LATCHES

P/O J1302 EXTERNAL CONNECTOR (FROM J-BOX)

REVERSE WILDCARD INPUTS (FROM EXTERNAL DEVICES)

INPUT 0 (+) 18 — JU67 — R1301 620 (SEE NOTE 1) — OPTO ISOLATOR U1306 — JU68 — +13.8V
INPUT 0 (-) 20 — JU58 — JU57 — C1306 .0068

INPUT 1 (+) 23 — JU65 — R1302 620 (SEE NOTE 1) — OPTO ISOLATOR U1307 — JU66 — +13.8V
INPUT 1 (-) 22 — JU60 — JU59 — C1307 .0068

INPUT 2 (+) 16 — JU69 — R1303 620 (SEE NOTE 1) — OPTO ISOLATOR U1308 — JU70 — +13.8V
INPUT 2 (-) 24 — JU62 — JU61 — C1308 .0068

INPUT 3 (+) 21 — JU71 — R1304 620 (SEE NOTE 1) — OPTO ISOLATOR U1309 — JU72 — +13.8V
INPUT 3 (-) 19 — JU64 — JU63 — C1309 .0068

STANDARD JUMPERING ALLOWS A REVERSE WILDCARD INPUT TO BE GENERATED WHEN THE EXTERNAL DEVICE PROVIDES A GROUND PATH VIA PINS 20, 22, 24, OR 19.

RESISTORS R1301-R1304 SHOULD BE SELECTED TO PROVIDE 20 mA THROUGH OPTO ISOLATOR. (U1306-U1309) WHEN ACTIVE.

U1310A INPUT PULSE LATCH: R1309 10K, R1305 10K, +5V, SD, CD, K, J, CP, Q, Q̄ → RWD 1 — JU42, JU41, RWD 1; JU39, SEE NOTE 2, JU40

U1310B INPUT PULSE LATCH: R1310 10K, R1330 10K, R1306 10K, +5V, CR1305, SEE NOTE 2 JU47, JU48 → RWD 2 — JU38, JU37, RWD 2

U1311A INPUT PULSE LATCH: R1311 10K, R1307 10K, +5V → RWD 3 — JU23, JU22, RWD 3; JU20, SEE NOTE 2, JU21

U1311B INPUT PULSE LATCH: R1312 10K, R1329 10K, R1308 10K, +5V, CR1306, SEE NOTE 2 JU24, JU25 → RWD 4 — JU19, JU18, RWD 4

DATA STROBE

CLEAR DATA

Q1305 TURNS ON WITH RESET BIT FROM MUXBUS

Q1305 M9706 — R1313 1 K — R1327 2.7K — R1328 10K — U1312D — R1326 47K — R1325 47K — +5V

U1303E

NON-INVERTING BUFFERS: U1303D, U1303C, U1303B

U1303A

U1301 1-8 ADDRESS DECODER: E3, A0, A1, A2, Q̄0–Q̄7 → A0–A7, E2, E1

U1302 1-8 ADDRESS DECODER: E3, A0, A1, A2, Q̄0–Q̄7 → A8–A15, E2, E1

JU108 SEE NOTE 7

CLEAR DATA SIGNAL WILL RESET THE DRIVERS U1313 AND U1314.

CLEAR DATA

U1312E

INHIBITS WRITING A BIT ON DATA BUS DURING RESET

NC — OPERATE — S1301 — RESET

DISABLES ALL SIGNALS FROM EXTERNAL DEVICES WHEN IN RESET.

U1305 WILDCARD ADDRESS DRIVERS: R1323 10K, MR, DO, D1, D2, D3, CP, Q0–Q3

FWA 1 — R1315 47K — JU8 SEE NOTE 3
FWA 2 — R1316 47K — JU107 SEE NOTE 7, JU9 SEE NOTE 3
FWA 3 — R1317 47K — JU110 SEE NOTE 3
FWA 4 — R1318 47K — JU108 SEE NOTE 7

REVERSE WILDCARD DATA BUS CONTROL GATE

U1315A: RWA1 — JU4 SEE NOTE 9 — JU3 SEE NOTE 3 — RWD1 — U1304B
U1315B: RWA 2 — JU5 SEE NOTE 9 — JU2 SEE NOTE 3 — RWD2 — U1304A
U1315C: RWA 3 — JU6 SEE NOTE 9 — JU1 SEE NOTE 3 — RWD3 — U1304D
U1315D: RWA 4 — JU7 SEE NOTE 9 — +5V — RWD4 — U1304C

REVERSE WILDCARD ADDRESS DRIVERS

DATA BUS CONTROL GAT... WILL WRITE A BIT ON D... WHEN THEIR OUTPUT(S... U1304 OUTPUTS ARE OF...